NAVAL POSTGRADUATE SCHOOL

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THESIS

PRELIMINARY DESIGN OF THE PANSAT ELECTRICAL POWER SUBSYSTEM

by

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June, 1990

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Preliminary Design of the PANSAT Electrical Power Subsystem

by

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ABSTRACT

This thesis presents a preliminary design of the electrical power system (EPS) for the Naval Postgraduate School's Petite Amateur Navy Satellite (PANSAT). The EPS is a photovoltaic silicon cell system consisting of solar array, batteries, battery charge regulator (BCR), and dc-dc convertors. The EPS provides power for up to two years of low earth orbit (480 km) operations. The solar array consists of 17 panels with thirty-two 2x4 cm solar cells in series on each panel. The cells have an efficiency of 14.3% and generate a panel voltage of 14.1 volts at beginning of life, providing an unregulated bus voltage of 13.5 volts. The bus voltage is clamped at a minimum 10.5 volts by two lead acid batteries in parallel with the bus. Each battery consists of five 2.1 volt, 5 ampere-hour lead acid cells and is capable of meeting mission requirements. The BCR monitors individual battery voltage, an indication of reserve capacity, and provides a pulse-modulated charge current alternately to each battery. The BCR is redundant with no single point of failure. Power conditioning for the unregulated bus is provided by redundant dc-dc convertors. The prototype BCR test results are presented along with alternative methods of increasing power output and efficiency.

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I. INTRODUCTION

A. PURPOSE

The purpose of this study is to provide a preliminary design for a prototype Electrical Power Subsystem (EPS) for the Naval Postgraduate School's low earth orbit (LEO) Petite Amateur Navy Satellite (PANSAT). The EPS includes the solar array, batteries, battery charging circuit (BCR), and power conditioning components required for operating the satellite payload and support equipment. Included in the study is the test and evaluation data on the BCR breadboard prototype and recommendations to improve system efficiency.

B. OBJECTIVES OF PANSAT PROJECT

Ojectives for the PANSAT project can be divided into two main categories, general project objectives and mission-specific objectives.

1. Project Objectives

The project objectives as defined by NPS's Space System Academic Group (SSAG) are [Ref. 1:p. 4]:

- Enhance the education of students in the space systems curricula by providing the opportunity for hands-on experience in a space systems design project.

- Provide a communications platform for the amateur radio community. This will provide a broad-based field of users for evaluation of satellite performance, as well as allowing the PANSAT project legitimate access to amateur UHF frequencies for experiments and telemetry.
- Provide a space-based platform for conducting experiments and monitoring satellite operations.

2. Mission Specific Objectives

The mission specific objectives for the PANSAT are:

- Design a low cost satellite bus capable of operating in LEO for at least 2 years.
- Test a spread spectrum, two-way communications package capable of communicating with users via a portable terminal.
- Data collection and validation for a solar cell parameter measurement experiment. Originally an experiment for annealing radiation damaged solar cells was planned, but the PANSAT's anticipated low altitude orbit precludes performing this experiment so the solar cell parameter measurement experiment was substituted.

C. BACKGROUND

The first small, low-cost LEO communications satellite was launched in December of 1961. The satellite, OSCAR 1

(Orbiting Satellite Carrying Amateur Radio), was a simple beaconing system built by amateur radio operators and operated on a battery pack for 400 hours. OSCAR 3, launched in 1965, provided two-way links between amateur radio operators in the U.S., Canada, and Europe. Since 1965, numerous small satellites have been built by various organizations. The most successful, the Radio Amateur Satellite Corporation (AMSAT), is a non-profit organization formed in 1969 and is responsible for the OSCAR-series satellites. AMSAT personnel are amateur radio operators who generally work in the aerospace field, so the satellites built by AMSAT reflect a sophisticated approach to small satellite design. Latter OSCAR-series satellites maintain a high degree of autonomous operation with an operating life of 5 years. The satellites are powered by solar arrays coupled with rechargeable nickel cadmium (NiCd) batteries. Magnets provide two-axis stabilization, allowing the spacecraft to align itself with the earth's magnetic field. OSCAR 10, AMSAT's most complex satellite, was designed for long life and high altitude orbits. The satellite was equipped with an apogee kick motor (AKM) and used spin stabilization. [Ref. 2:p. 82]

As interest in small satellites has increased, the competition for free launch services has also increased. AMSAT used a modular approach for designing the next generation of OSCAR satellites aimed at minimizing size and mass. The Microsat OSCAR-series is a small 10 kg digital

store-and-forward satellite composed of 5 individual stacked modules, each performing a separate function. The power module uses high-efficiency silicon cells and rechargeable NiCd batteries providing 8 watts (orbit average) of power. The satellite's CPU monitors and maintains the optimum output from the solar array. In 1989, three Microsats were successfully launched from an Ariane booster. [Ref. 3:p. 39]

Recently, the Defense Advanced Research Projects Agency (DARPA) began developing a lightweight LEO satellite bus. A small satellite offers a platform for various military applications which include store-and-forward communications, remote imaging, intelligence gathering, data relay for oceanographic and meteorological buoys, nodes for C^3 networks, generation and distribution of global databases, and intrafleet or intratheater communications. [Ref. 4:p. 48]

In 1987, the NPS's SSAG developed the Orion mini-satellite in response to military and commercial demands for a low-cost satellite bus capable of supporting small innovative payloads and experiments. The Orion satellite bus is fully autonomous providing telemetry, attitude control, orbital boost/station keeping, electrical power, microprocessor and data storage for up to 22.5 kg of user payload. Orion is equipped with a hydrazine propulsion system, which can boost the satellite into a 1460 km circular or 4020 km elliptical orbit from an initial orbit of 245 km. [Ref. 5:p. 7]

Although Orion's projected 1.5 million dollar budget is small in comparison to large satellites, its cost and complexity are negative factors in the SSAG's first attempt to build and launch a satellite. As a prelude to the Orion project, the PANSAT is being developed at a projected lower cost of 150,000 dollars for hardware and with less complexity [Ref. 1:p. 3]. The design, fabrication, and testing of PANSAT will be performed at NPS in order to minimize cost.

D. PRELIMINARY DESIGN CONSIDERATIONS

1. PANSAT Specifications and Power Requirements

The Naval Postgraduate School's Space System Academic Group (SSAG) provided the following specifications and requirements [Ref. 6]:

- The PANSAT configuration, depicted in Figure 1, is a small tumbling communications satellite.
- PANSAT's shape is a polyhedron with twenty six sides. Eighteen sides are 8.4 x 8.4 cm squares and the remaining eight sides are 8.4 cm equilateral triangles.
- The satellite will be injected into low earth orbit from a Get Away Special (GAS) cannister mounted in the space shuttle bay.
- PANSAT should cost between $100,000 - $150,000.
- Desired launch date within 2 years (October 1991).

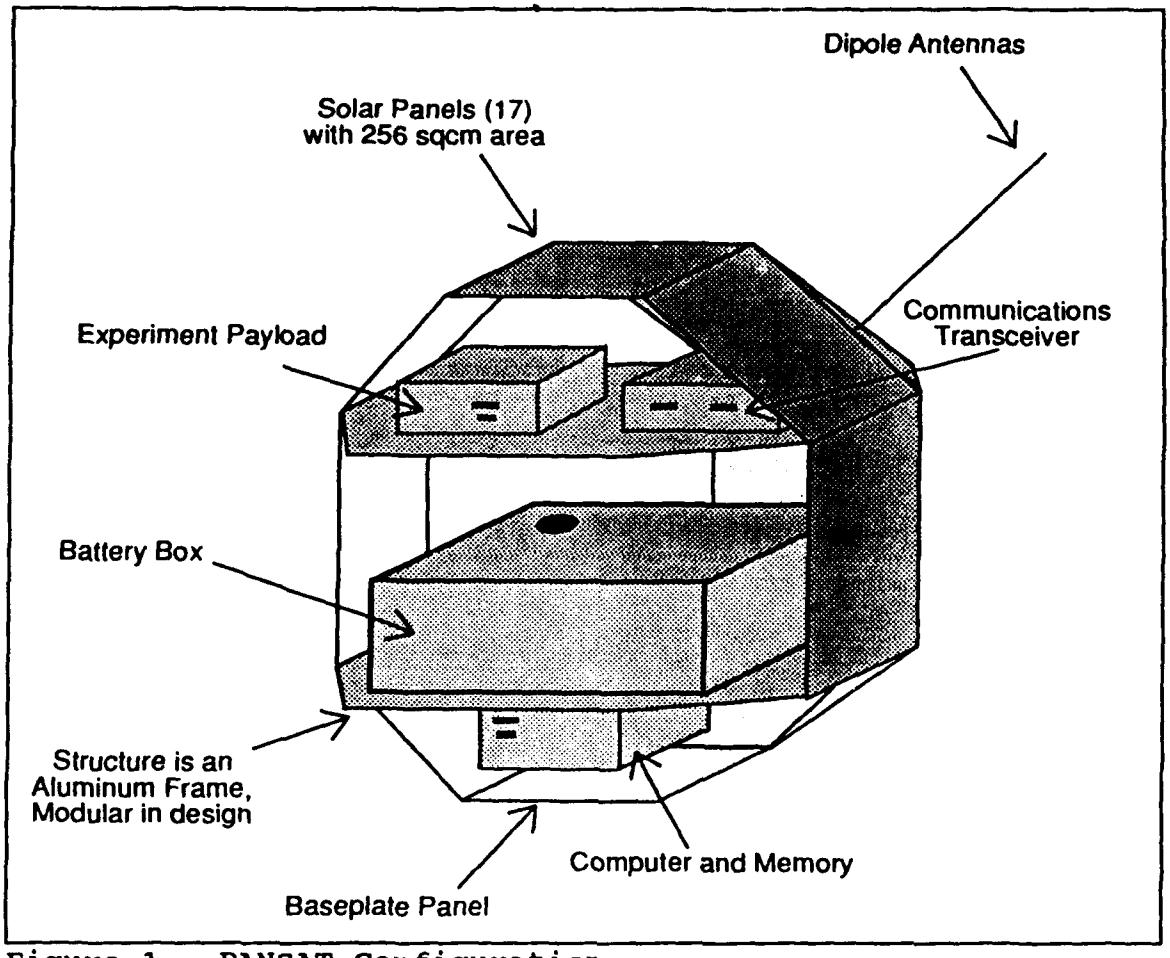

Figure 1. PANSAT Configuration

- PANSAT should be designed for a 2-year operating life.
- 17 panels (18.4 cm x 18.4 cm) are available for solar power generation. The eighteenth square panel, the baseplate panel, is for mounting the PANSAT in the GAS cannister.
- The satellite's microprocessor requires 2.6 watts at +5 volts.

- The experimental payload will require 0.5 watts or less at +5 volts.
- The EPS should be capable of delivering a minimum of 15.7 watts of peak power for 24 minutes to the transmitter.
- The receiver will be on continuously and will require approximately 2 watts.

2. Priority of Design Criteria

The most important factors or criteria used in designing the PANSAT EPS are listed below in descending order according to their impact on system design:

- **Reliability** - Reliability of the EPS is considered tantamount in the EPS design. If possible, the design should avoid any possible single point failures in the EPS, which would jeopardize satellite operations.
- **Simplicity** - Simplicity in the EPS design is desired for several reasons. First, the more complicated the EPS design, the more likely development and system integration time will lengthen, thereby setting back the desired launch date. Furthermore, the cost of the EPS will rise and a degradation in reliability or the possibility of a single point failure becomes probable. Finally, simplicity in design is

desirable, because the transient nature of personnel (students) involved on the PANSAT and the small number of NPS staff assigned to the project.

- **Cost** - Cost is a major consideration. The projected budget for PANSAT is exceedingly low. Certain types of solar cells or batteries suitable for PANSAT could easily cost as much as the entire project.
- **Efficiency** - While high efficiency is desired, it is less of a consideration than reliability, simplicity, or cost.
- **Weight** - Weight is not considered to be a design issue. The maximum weight the GAS cannister can accommodate is 68.0 kg (150 lbs) excluding the ejector mechanism. [Ref. 6]. A satellite's EPS typically comprises 26% of the satellite's dry weight [Ref. 7:p. 391]. PANSAT's EPS mass should be less than 17.7 kg. Initial calculations using the power budget described below and the heaviest space-rated battery, NiCd, still place the EPS weight under this value.

3. Baseline Satellite Models

Two satellites, Northern Utah Satellite (NUSAT) and Global Low Orbiting Message Relay Satellite (GLOMR), were

selected as baseline models for design comparison to the PANSAT. Both were low budget tumbling communications satellites placed in LEO from a space shuttle GAS cannister.

a. **NUSAT**

NUSAT was a small, 48 kg, 26-faceted polyhedron, placed in a 360km circular orbit in April of 1985. The satellite was built by Utah State University and Weber State College for the purpose of testing the shuttle GAS cannister as a platform for ejecting small satellites into independent orbit. Additionally, NUSAT had a L-band measurement system for determining the vertical radiation pattern of air traffic control radar antennas. [Ref. 8:p. 63]

NUSAT's EPS consisted of 12 solar panels wired in parallel to a 5 cell lead acid battery feeding an unregulated bus. Each solar panel had 28 2x4 cm silicon solar cells connected in a single series string. Each cell in the lead acid battery was rated at 2.1 volts, 5 ampere-hours providing a battery voltage of 10.5 volts. The unregulated bus varied between the battery voltage and solar array voltage, approximately 10.5 to 13.5 volts. Power conditioning was provided by one +5 volt switch regulator and three +/-5 volt dc-dc converters. [Ref. 9:p. 92] NUSAT's 10-watt transmitter used unregulated bus voltage [Ref. 10:p. 30].

b. GLOMR

GLOMR was a 64.5 kg, 62-faceted polyhedron low orbiting satellite capable of two-way packet data relay communications. The satellite was built by Defense Services Inc. (DSI) for the purpose of demonstrating the feasibility of a low-cost LEO store-forward, two-way, digital communications satellite. The satellite was built in one year for under one million dollars. GLOMR was injected into a 57° 322 km circular orbit in October of 1985. The satellite's on-orbit life of 421 days exceeded the initial prediction by NASA of 200 days. Hardware performance met or exceeded design expectations with no operational malfunctions. [Ref. 11:p. 1]

GLOMR's EPS consisted of 30 solar panels, feeding an unregulated bus with lead acid batteries for peak demand and eclipse periods. Each solar panel contained 18 2x4 silicon cells with an output voltage of 8.5 volts. Twelve Gates "D" lead acid batteries, each rated at 2.0 volts at 2.5 ampere-hours, were used. The cells were connected in four parallel sets of three cells in series providing an output of 6.0 volts at 10 ampere-hours. The unregulated bus was allowed to vary between 6.0 and 7.5 volts. [Ref. 12]

E. ASSUMPTIONS IN DESIGN PROCESS

The PANSAT concept is still evolving with parallel design proceeding on key subsystems. This has resulted in a lack of definition on power requirements and conditioning for the EPS.

as a result, numerous assumptions must be made in completing a prototype EPS. Minor assumptions are discussed in the applicable sections of this thesis and the most important assumptions are listed below.

1. PANSAT Communication Operations

The PANSAT's transmitter can be operated at any time in the satellite's orbit. Although the batteries are capable of supplying power to the transmitter during eclipse, it is not desirable due to the greater depth of discharge (DOD) on the batteries. A greater DOD reduces the life expectancy of the batteries and, if repeated often enough, could shorten PANSAT's operating life.

2. Orbital and Eclipse Period

PANSAT's orbital period, τ_p, is defined by

$$\tau_p = \frac{2\pi}{60}\sqrt{\frac{a^3}{\mu}} \qquad (1.1)$$

where

τ_p = orbital period (min),

α = earth's radius + orbit altitude (km), and

μ = 398601.2 km^3/s^2.

The period of eclipse is expressed as:

$$\tau_e = \frac{\tau_p}{\pi} \cos^{-1}\left(1 - \frac{r_e^2}{a^2}\right)^{1/2} \qquad (1.2)$$

where

τ_e = eclipse period (min) and

r_e = earth's radius (km).

Table 1 shows the orbital and eclipse periods for various PANSAT orbits using a shuttle launch.

TABLE 1. PANSAT ORBITS

Orbital Altitude (km)	Orbital Period (min)	Eclipse Period (min)
160	87.7	37.6
200	88.5	37.3
250	89.5	36.9
300	90.5	36.6
350	91.5	36.3
400	92.6	36.1
480	94.2	35.8

At an orbit of 480 km, PANSAT will have an orbital period of 94.2 min with a eclipse time of 35.8 min. This is the worst-case condition for the EPS since the solar array output, based on initial calculations, cannot meet the estimated peak load demands. Also, a two-year operational life requires an orbital injection at higher altitudes where the orbital decay is less. Finally, solar cell degradation

due to radiation, although small, will be greater at higher orbits.

3. Tumbling Rate

PANSAT orbital injection from the shuttle GAS Cannister will be accomplished using a spring ejector mechanism. It is assumed that the spin or tumble rate induced will be small, approximately 0.1 radians/sec, and favor no particular axis [Ref. 13 p. 6].

4. Thermal Control

PANSAT's thermal control system will utilize passive measures to maintain the satellite's environment within acceptable limits. Table 2 lists the minimum and maximum design temperatures during periods of operation and nonoperation [Ref. 14:p. 266]. Additionally, the EPS components should be capable of withstanding worst case

TABLE 2. PANSAT DESIGN TEMPERATURES

EPS Component	Design Temperature (°C)	
	Nonoperating	Operating
Electronics	-30/+55	+10/+45
Batteries	-10/+25	0/+45
Solar Array	-160/+80	-160/+80

exterior temperatures of -160°C to 100°C while stored in a GAS cannister in the orbiter bay. Container insulation, conductive resistance, and PANSAT's passive thermal control

measures should ensure these extreme temperatures are not experienced. [Ref. 15:p. 65]

5. Power Budget

Designing and maintaining a positive power budget cannot be overstressed. When a satellite has a negative power budget, power is used faster than the solar cells can recharge the batteries, obviously impacting operations. OSCAR-12, built by the Japanese segment of AMSAT, has a negative power budget due to an overestimate of battery capacity and solar array efficiency. In the past three years, following its launch, OSCAR-12 has been limited in operations and accessability by users. [Ref. 16]

An estimate of PANSAT's power budget is listed in Table 3. The power requirements for the microprocessor, transmitter, receiver, and payload are part of the design requirements. Power requirements for power conditioning reflect conditioning of the payload and microprocessor using convertors with an 85% efficiency. The BCR is assumed to draw an average of one watt. This value accounts for power required by the BCR circuit and ineffciencies in the battery charging process. Table 3 lists average power usage over one orbital period in terms of watts and watt-hours. Any deficit in the power budget during peak operations will have to be supplied by the batteries. A 10% margin is provided to ensure the EPS is capable of continuously providing the power required by

PANSAT subsystems and payload. The margin also allows for growth in the EPS design process. The minimum power requirements for satellite operations during eclipse are presented in Table 4. The eclipse power requirements are listed in terms of watt-hours used by the microprocessor, receiver, and for power conditioning. PANSAT's batteries will supply satellite subsystem power during eclipse. Power requirements for a heater element capable of maintaining environmental temperatures within battery limits has not been addressed. GLOMR was equipped with four 5-watt heaters which could raise the internal temperature, if needed, by 10°C. However, the satellite temperature was warmer than expected and the heaters were not used [Ref. 11:p. 4]. NUSAT was not equipped with heaters and experienced no system degradation due to low temperatures during eclipse. It seems reasonable to assume that PANSAT will not require a heater for the current mission profile. However, if a heater should be added at a later date, the available transmitter power may have to be reduced depending on the output of the solar array.

TABLE 3. PANSAT POWER BUDGET

SATELLITE COMPONENT	NOMINAL PWR (W)	DUTY CYCLE (%/ORBIT)	AVERAGE PWR (W)	AVERAGE WATT-HR
Microprocessor	2.6	100.0	2.6	4.1
Transmitter	15.7	25.5	4.0	6.2
Receiver	2.0	100.0	2.0	3.1
BCR	1.0	62.0	0.6	0.9
PWR Conditioning	0.5	100.0	0.5	0.8
Payload	0.5	62.0	0.3	0.5
POWER/ORBIT	-	-	10.0	15.7
10% Margin	-	-	1.0	1.6
TOTAL POWER	-	-	11.0	17.3

TABLE 4. ECLIPSE POWER REQUIREMENTS

SATELLITE COMPONENT	POWER (W) PER ECLIPSE	WATT-HR PER ECLIPSE
Microprocessor	2.6	1.6
Receiver	2.0	1.2
PWR Conditioning	0.5	0.3
TOTAL POWER	5.1	3.1

II. OVERVIEW OF ELECTRICAL POWER SYSTEM (EPS)

A. POWER SYSTEM CONFIGURATION

Three power systems topologies for the PANSAT were considered. They are [Ref. 7:p. 393]:

1. Unregulated bus

Figure 2 depicts a simplified block diagram of an unregulated bus. The solar array and batteries are connected directly to the distribution bus, allowing the bus voltage to float between the solar array and battery voltages. During sunlight operations, the solar array determines the voltage of the distribution bus. When the satellite is in eclipse, the distribution bus assumes the value of the battery voltage. During peak power demands, when the power capability of the solar array is exceeded, the bus voltage drops and is clamped at the battery voltage by a forward-biased diode. A small secondary solar array in series with the primary array is activated, as needed, to charge the satellite batteries. A control unit positions two switches, shown in Figure 2, which determine battery charge and discharge. The primary disadvantage of an unregulated bus is that the bus voltage is determined by the electrical characteristics of the solar array and batteries. The solar array's electrical characteristics vary due to load demands, operating

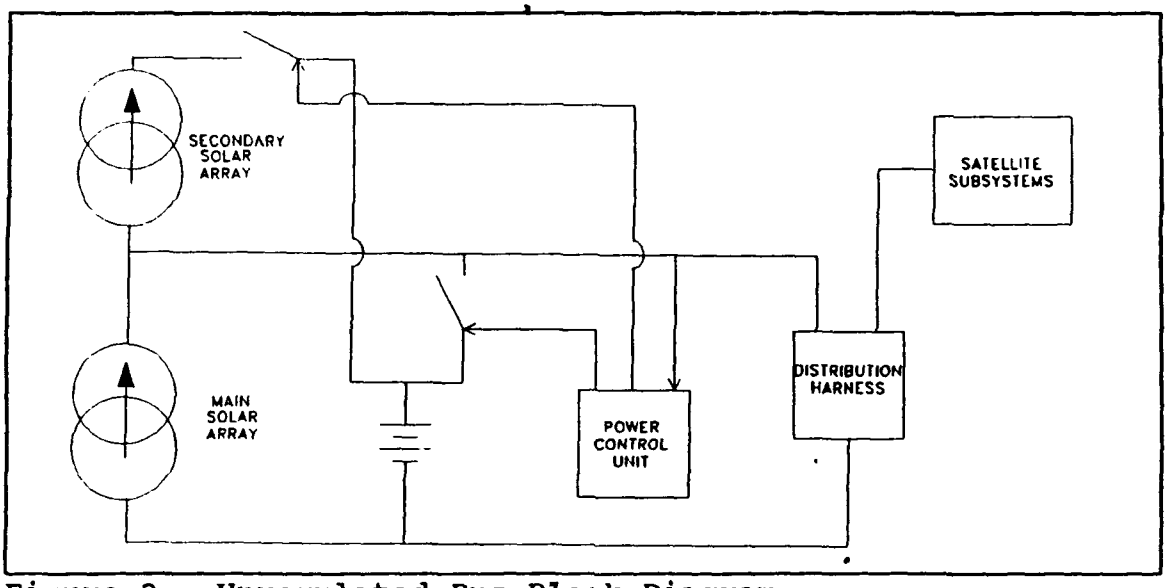

Figure 2. Unregulated Bus Block Diagram

temperature, variations in solar intensity, and degradation from radiation. As a result, large voltage variations in the distributed bus can occur. The unregulated bus topology is the most widely used in satellite design because of its simplicity in hardware requirements.

2. Sunlight-Regulated Bus

A sunlight-regulated bus is similar to the unregulated bus above, except large voltage variations are minimized by maintaining the operating point of the solar array at a set value by means of a shunt, series, or pulse-width modulated regulator. Figure 3 depicts a block diagram of a sunlight-regulated bus. A battery charge regulator and a discharge diode replace the two switches in Figure 2. A control unit adjusts the solar array regulator and is dissipated thereby maintaining the solar array voltage at a fixed value. Thus,

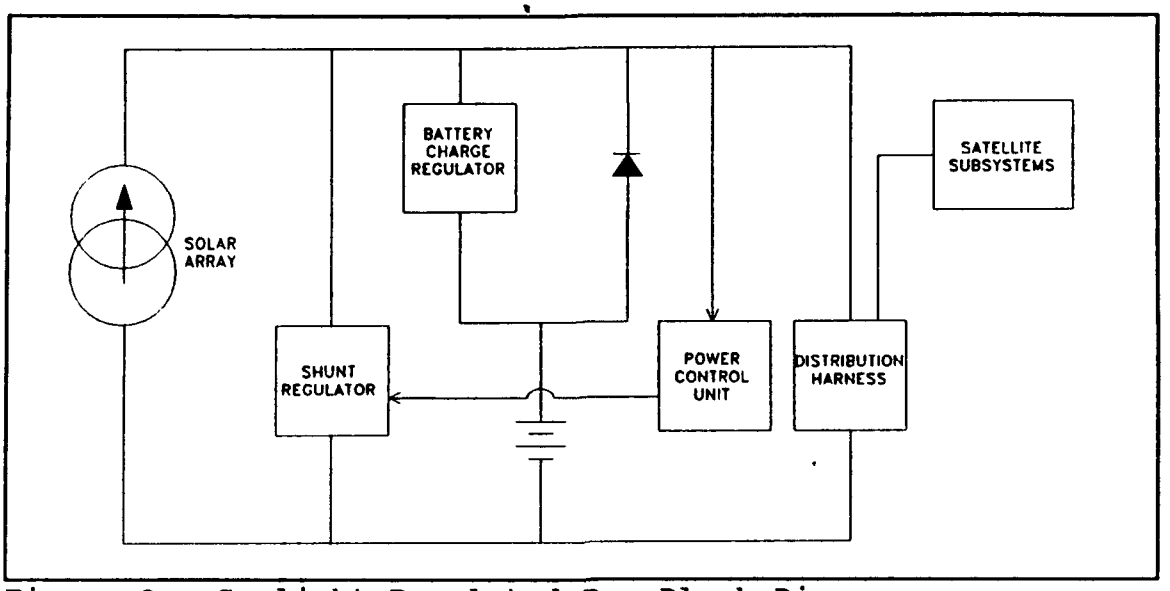

Figure 3. Sunlight-Regulated Bus Block Diagram

voltage variations are reduced where hardware requirements and complexity are increased. A disadvantage of the sunlight-regulated bus, and the unregulated bus to a lesser extent, is the occurrence of a condition known as "lock-up" where the solar array output locks to a set of stable conditions which are less than optimum. This phenomenon is beyond the scope of this thesis and is left for further investigation.

3. Regulated Bus

The regulated bus, Figure 4, decouples the energy source from the distribution bus providing stable voltage regulation during both sunlight and eclipse periods. The solar array voltage is maintained by the solar array regulator in sunlight conditions and a battery discharge regulator maintains the bus distribution voltage during eclipse, instead of switches or discharge diodes. The disadvantages of a

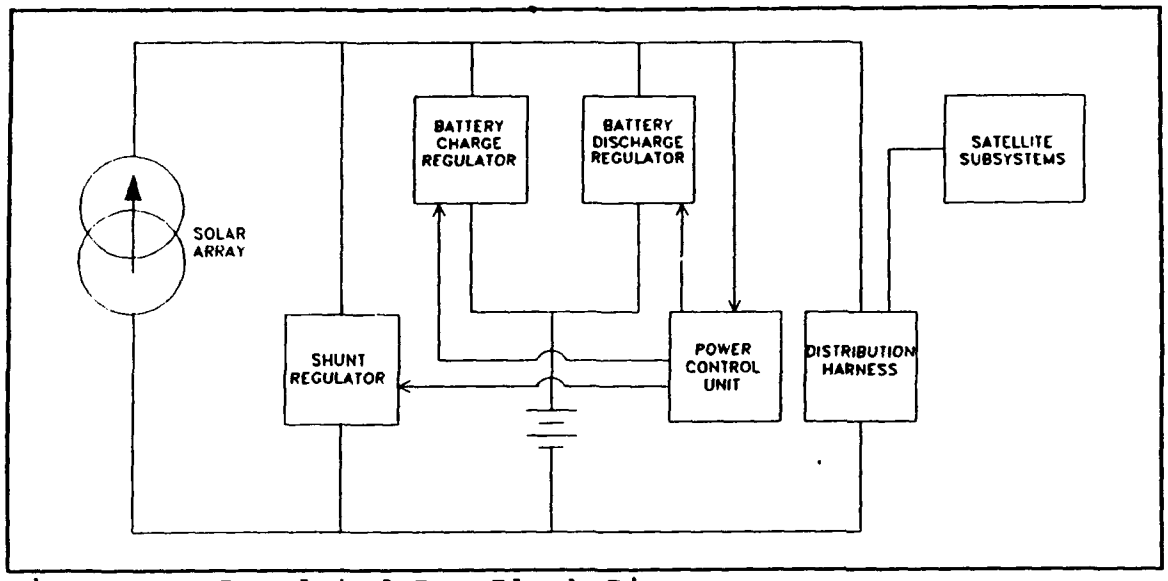

Figure 4. Regulated Bus Block Diagram

regulated bus are: an increase in hardware, a decrease in efficiency caused by the battery discharge regulator, and an increase in thermal dissipation.

B. DECENTRALIZED VS CENTRALIZED BUSES

Regardless of the bus topology selected, regulated or unregulated, PANSAT's subsystems will require different voltages with varying regulation requirements. Therefore, the distributed bus voltage will require further regulation using regulators and dc-dc convertors. There are two forms of regulation this process can take, centralized or decentralized. In a decentralized bus, regulation is carried out at each load separately. The advantage of a decentralized regulation system is that each subsystem power requirement can be met without compromise to another subsystem. A centralized

regulation system provides voltages which are a compromise for all subsystem requirements. The chief advantage of centralization is a reduction in the number of regulators and dc-dc convertors required. [Ref. 17:p. 148]

The decentralized regulation concept is particularly attractive for the PANSAT EPS for several reasons. First, since the PANSAT is not a fully mature design, it is anticipated that user power requirements will change as the design evolves. A decentralized approach allows a specific subsystem demand to be modified by simply changing the subsystem's convertor without altering anything else. Secondly, the primary power requirement is from PANSAT's communications subsystem which can probably use unregulated bus voltage. This reduces the need for power conditioning making a decentralized system more practical.

C. PANSAT EPS FUNCTIONAL DESCRIPTION

A modified unregulated bus topology is selected for the EPS based on its simplicity and efficiency. A modification to the unregulated bus concept is the deletion of a secondary solar array for charging PANSAT's batteries and the addition of discharge diodes for battery discharge. PANSAT's random tumbling and small surface area precludes using a secondary solar array battery charging scheme. Figure 5 is a functional block diagram of the PANSAT EPS. The battery discharge block is realized by a forward-biased diode, one for each battery.

The two switches in Figure 5 are microswitches that isolate the batteries and solar array prior to launch. The use of a shunt regulator for PANSAT's EPS was examined and rejected because of the increased complexity. Instead, the satellite solar panel voltage and the battery voltage are selected close enough to minimize large voltage variations. The main functional components of PANSAT's EPS are:

1. Solar Array

A solar array is a group of solar cells which produce electrical energy from the photovoltaic conversion of solar energy. Voltage and current output of the array are determined by the number of cells in series and parallel, respectively. Each of the 17 solar panels is connected in parallel with each other via blocking diodes, making the solar array voltage equal to the panel voltage. Solar cells are made from various types of semiconductor materials such as silicon, gallium arsenide (GaAs), and more recently indium phosphide. Currently, silicon is the predominant solar cell used in space applications and is also the least expensive.

PANSAT's solar array consists of 544 silicon cells. Although GaAs cells are more efficient than silicon, their cost is five to ten times more. Initial calculations indicated GaAs cells for PANSAT could cost as much as 136,000 dollars. This was for the bare solar cell and did not include covers or mounting. Obviously, cost was a major factor in

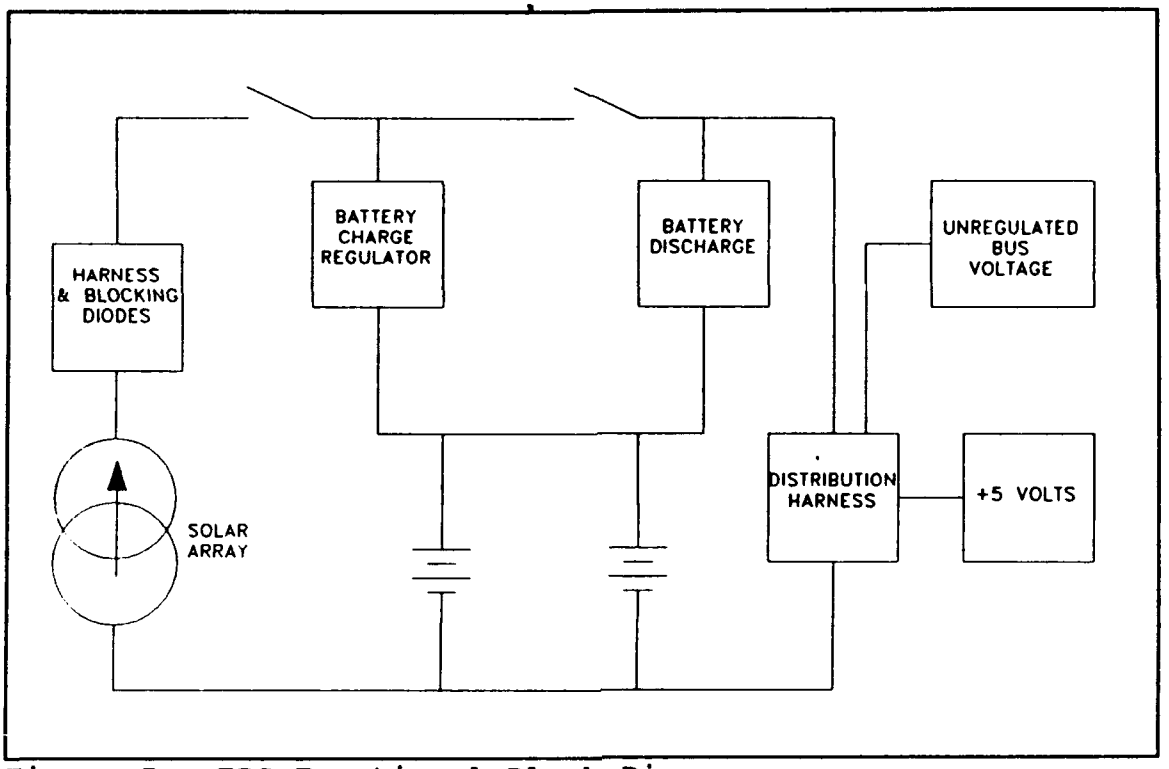

Figure 5. EPS Functional Block Diagram

rejecting GaaS cells for PANSAT. Indium phosphide cells were also considered and rejected due to cost.

PANSAT's solar array panels can accommodate 32 2x4 cm cells or 64 2x2 cm cells. A typical silicon solar cell generates approximately 0.46 volts at maximum power regardless of the surface area of the cell. Therefore, PANSAT's array is capable of providing an approximate panel voltage of 15 or 30 volts at 28°C. A panel voltage of approximately 30 volts yields too large a voltage difference between battery voltage and the array, so a solar array voltage of approximately 15 volts at 28°C was selected. This voltage will be degraded by

several volts due to the increased operating temperature of the solar cells.

2. Batteries

PANSAT's unregulated bus will be clamped at a nominal 10 volts by two batteries hard-wired in parallel with the solar array and load. Each battery is of sufficient capacity to meet all mission requirements if the other battery should fail. The battery voltage is selected several volts below the solar array voltage to ensure that sufficient potential exists to drive current into the batteries during charging conditions. At the same time, the battery voltage is close enough to the solar array voltage to prevent large fluctuations in bus voltage between periods of eclipse and sunlight. A pulse-modulated BCR alternately charges each battery as required.

Consideration was given to having only one battery supply the load while the second battery was brought off-line for charging. After the on-line battery discharged to a preset level of depth-of-discharge (DOD), the batteries would be switched allowing measurement of open circuit voltage and a determination of the batteries' true capacity. This design offered no major advantage over the one selected other than measuring battery capacity. The DOD and battery life expectancy, for both methods, are approximately the same. Taking a battery off-line would require fail-safe protection

in the event the on-line battery developed a shorted or open cell. Keeping the batteries hard-wired in parallel is the simplest, most reliable method.

3. Pulse Modulated BCR

Pulse modulation of the battery charging circuit serves several purposes. First, since only one battery is being charged at a time, a battery with a weak or shorted cell will not deprive the good battery of its allocated share of charging current. Without a pulse modulation scheme, if a battery cell shorts, the battery voltage drops from 10 volts to 8 volts while the good battery voltage remains at 10 volts. Hence, the 8 volt battery will draw more charging current than the 10 volt cell. Secondly, pulse-modulation allows the BCR circuit for the two batteries to be totally redundant and independent. Finally, alternating the charging of each battery prevents excessive power drains on the EPS when other subsystems are being used.

4. Power Conditioning

PANSAT will use off-the-shelf dc-dc convertors for voltage and power regulation as required. As previously mentioned, the transmitter and receiver will use unregulated distribution bus voltage. This scheme has been successfully employed by the OSAR series, GLOMR, and NUSAT satellites.

D. EPS ACTIVATION AND OPERATION

1. Activation

Redundant hermetically-sealed microswitches are mounted on the PANSAT's baseplate panel, isolating the fully charged batteries from the solar array and distribution bus prior to PANSAT's orbital injection. Upon ejection from the GAS cannister, the microswitches close connecting the batteries to the solar array and distribution bus andactivating the satellite's subsystems. Parallel redundancy of each switch ensures proper activation of the EPS. The microswitches are sealed to preclude sparking in the event of a battery leak in the enclosed atmosphere of the GAS cannister which could cause an explosion. [Ref. 18:p. 286]

2. Operation

PANSAT's EPS has two modes of operation, one for non-eclipse periods and the other for eclipse.

a. EPS Non-eclipse Operation

During non-eclipse periods, power is provided directly to the satellite subsystems from the illuminated solar array. The transmitter and receiver will use the unregulated solar array voltage minus diode voltage drops. Subsystems requiring power conditioning will receive their power via dc-dc convertors. Anytime the load demand exceeds the output of the solar array, when all subsystems are on-line simultaneously, the solar array voltage will drop until its

value is equal to the battery voltage. The battery voltage will then clamp the distributed bus voltage until the battery voltage begins to decrease because of a reduction in battery capacity. To prevent a total depletion of battery capacity, a transmitter lockout will be required to inhibit transmitter operation by amateur radio operators until the batteries are sufficiently recharged. The transmitter lockout should be capable of being overridden by ground-controllers.

b. EPS Eclipse Operation

When PANSAT enters eclipse, illumination of the solar array panels cease and the BCR stops operating. The battery voltage becomes the bus voltage and supplies power to the receiver, microprocessor, and transmitter. If the transmitter is not operated during eclipse, the batteries' DOD will be slight. PANSAT's batteries are sized to provide sufficient capacity for operating the transmitter at peak power in eclipse. This will cause a considerably higher DOD and will require larger periods of battery charging after the satellite leaves eclipse. Since the battery voltage is close to the solar array panel voltage, efficiencies for dc-dc convertors during eclipse should approach those during non-eclipse periods. The BCR is reactivated when PANSAT exits eclipse.

E. EPS HARDWARE SELECTION

1. Advantage of CMOS Devices

The amount of power available for satellite housekeeping functions is limited and power requirements in support of PANSAT's EPS should be kept to a minimum. The complementary-symmetry metal-oxide semiconductor (CMOS) family is an ideal selection for PANSAT's EPS. CMOS devices require less power than transistor-transistor logic (TTL) and the input current required by a gate is small, 1 pA or less. The output current, at least 1 mA, is much larger than the input current. This allows for a large fan-out limited only by the propagation delay time. [Ref. 19:p. 89]

CMOS 4000 B-series devices have a recommended supply voltage of 3 to 18 volts [Ref. 20:p. 44]. Since the nominal output of PANSAT's solar array is 15.0 volts, the supply voltage for the BCR's CMOS and CMOS-compatible devices can be taken directly from the unregulated solar panel voltage, after the panel's blocking diode.

An additional advantage of CMOS components is their low power dissipation [Ref. 21:p. 3]. This reduces the satellite's thermal control problem by minimizing thermal energy generated by PANSAT's electronic circuits.

2. Radiation Effects on EPS Hardware

PANSAT's proposed low earth orbit is a relatively benign environment insofar as radiation degradation to

electronic hardware is concerned [Ref. 22]. Several Oscar series satellites launched into low altitude orbits have used some commercial-grade electronic components with no detrimental effects on mission performance [Ref. 23]. Radiation hardening should not be a factor in selecting EPS hardware.

3. Quality and Reliability

PANSAT's EPS, for the purpose of selecting reliable components, can be broken into three distinct categories: integrated circuits, discrete components, and the solar array hardware. Selection of military-rated hardware will ensure quality components with a low probability of failure. A brief discussion of the quality-assurance documents which cover these categories follows.

a. Integrated Circuit Reliability Ratings

Two basic documents govern the testing and quality of integrated circuits, MIL-M-38510 and MIL-STD-883. MIL-M-38510 outlines all of the screening, electrical test, qualification, quality conformance and certification requirements for integrated circuits. Appendix A of MIL-M-38510 outlines the minimum quality assurance procedures required [Ref. 24:p. 1]. MIL-STD-883 provides established procedures for carrying out testing delineated in MIL-M-38510. It standardizes integrated circuit screening flow which achieves an in-equipment failure rate of 0.08% per thousand

hours for Class B and 0.004% for Class S [Ref. 24:p. 18]. Class S devices are intended for space flight application while Class B devices are used primarily for aircraft and ground systems. Class S procedures and requirements appear to parallel those of Class B, but there are variations in the handling and processing which make Class S devices exceptionally high in reliability and quality [Ref. 24:p. 34]. Both Class S and Class B testing rely heavily on burn-in as a key determinant of reliability. Although Class S is more desirable for PANSAT components, Class B are acceptable if the cost difference is too high. Both classes are hermetically sealed and have a temperature rating of -55°C to 125°C.

b. Discrete Component Reliability Ratings

MIL-S-19500 is the discrete component testing and certification document equivalent to MIL-M-19500 for integrated circuits. MIL-S-19500 is a standardized specification for controlling the reliability and product assurance of discrete semiconductor products. MIL-STD-750, the discrete component equivalent of MIL-STD-883, provides detailed test methods for implementing MIL-S-19500. There are four levels of products delineated by MIL-S-19500. They are JAN, JANTX, JANTXV, and JANS. The differences in the categories are based on differences in reliability levels for various systems. JAN designated components are unscreened and are not appropriate for the PANSAT. The JANS category are

highly tested and suitable for space or critical component applications. JANTX and JANTXV devices are designed for higher radiation environments but are not as reliable as JANS devices. The JANS rating requires a longer burn-in compared to JANTX and JANTXV. Temperature ratings, except JAN, are similar to Class S and Class B for integrated circuits. While the JANS rating is desirable for PANSAT discrete semiconductor components, JANTX and JANTXV devices are acceptable replacements. [Ref. 24:p. 80]

Discrete non-semiconductor components such as capacitors and resistors are discussed in MIL-C-39003 and MIL-R-39008, respectively.

c. **Solar Array Design Specifications**

MIL-S-83576 establishes the general design, fabrication, performance, and testing requirements for solar arrays [Ref. 25:p. 1]. Although PANSAT's solar array does not require adherence to military specifications, it is recommended that applicable portions of MIL-S-83576 be followed in construction and assembly of the solar panels to avoid panel failures or poor performance.

III. SOLAR CELL ARRAY DESIGN

A. SOLAR ARRAY DESIGN CONSIDERATIONS

Solar array design is both an analytical and iterative process to determine the physical and electrical properties of the solar cells at BOL and EOL. In the interest of brevity, a discussion of solar cell theory is not included in this thesis. The reader is referred to Chapter 6 of Reference 14 for a brief introduction to solar cell theory and design. A more indepth discussion of solar cells can be found in Chapter 3 of Reference 26. Calculations performed in this chapter use standard Jet Propulsion Laboratory (JPL) solar array design methods from Chapter 12 of Reference 26. The design process is reversed in that the number of cells required for the solar array, both parallel and series, are already known. Calculations of satellite eclipse exit temperature, power output after eclipse, and power output at equinox are not required for a preliminary design and are left for further investigation. The packing factor, the factor that accounts for intercell connection space, is not required for the preliminary calculations because the solar array's panel size is designed to accommodate 32 2x4 cm^2 cells. However, the packing factor was calculated at 0.95, which verifies that the panels are of sufficient size for the solar cells. The major

considerations in a preliminary design of PANSAT's solar array are:

- The average surface area available for generating solar power.
- Selection of a solar cell, cover, substrate and bonding agents.
- The power output of the solar array at the sun's lowest level of illumination, summer solstice.
- The radiation degradation on the solar array during PANSAT's two year mission.
- The EOL power output of the solar array at summer solstice.
- The minimum solar array panel voltage, at equinox, at the maximum power output of the solar array.
- A suitable solar panel blocking diode which minimizes forward voltage drop.

B. SOLAR ARRAY EFFECTIVE SURFACE AREA

An analysis was performed on the average effective surface area of PANSAT's solar array using the dynamic analysis program in Appendix A, provided by the NPS SSAG, and the following assumptions [Ref. 6]:

- The satellite's spin axis relative to the sun is random with no preferential direction.
- The rate of tumbling is uniform with each panel receiving equal exposure.

The program, corrected for angle of incidence, calculates the solar array effective surface area using a satellite rotation of 0.1 Rad/sec about the x-axis and an initial reference angle for the z-axis of 0° to 30°. The program samples the solar array surface area every second for one satellite rotation. These samples are then averaged, by hand, to determine the average area for the given initial reference angle. The coordinate system's origin is at PANSAT's center and the z-axis is normal to the base plate panel, bisecting both the base plate panel and the opposing solar panel. The x and y axis are defined by the right-hand cartesian coordinate system. Due to PANSAT's symmetry, variation of the reference angle allows the effective surface area to be calculated for any axis of rotation. For initial reference angles greater than 30° the data is repeated. Table 5 lists the average effective surface area for one cycle, starting with an initial reference angle of 0° and increasing in 5° increments to 30°. Analysis of the data indicates the worst or minimum average surface area is with a 0° reference angle. Figure 6 is a plot of the surface area for a period of 63 seconds, one cycle of rotation. The low surface area value at 47 seconds in Figure 6 is caused by the baseplate panel used for mounting the satellite in the GAS cannister. This panel is not a power generating surface and, at 47 seconds, is normal to the sun reducing the solar array area being illuminated. In other words, the minimum surface area for the solar array occurs

when the satellite is tumbling such that the baseplate panel is fully illuminated and normal to the sun during a portion of each rotation cycle. The average value of 1145 cm^2, with the baseplate normal to the sun, is used as the effective surface area of the solar array for design calculations.

TABLE 5. AVERAGE EFFECTIVE SURFACE AREA

Reference Angle	0°	5°	10°	15°	20°	25°	30°
Average Area (cm^2)	1145	1195	1222	1244	1261	1272	1271

C. SOLAR CELL SELECTION

To narrow the field of solar cells considered, a determination must be made of the minimum solar cell efficiency which will satisfy PANSAT's power budget. The efficiency of an individual solar cell is defined as [Ref. 26:p. 3.2-2]

$$\eta = \frac{P_o}{P_I} = \frac{P_o}{(p_i)(A_c)} \qquad (3.1)$$

where

P_o = power output of the cell,

P_I = energy input to the cell,

p_i = solar illumination level per unit area, and

A_c = active solar cell area upon which solar energy is incident.

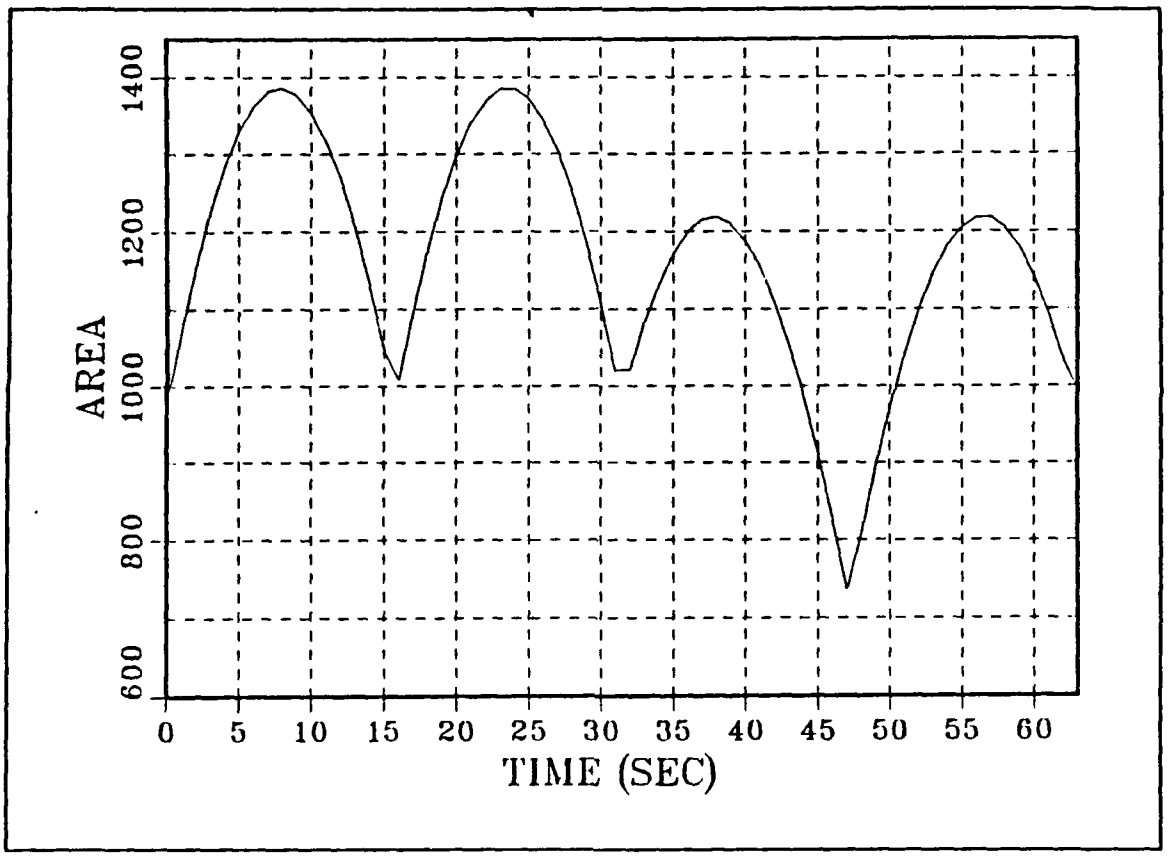

Figure 6. Minimum Effective Surface Area

Modifying Equation 3.1 to reflect the total power of the solar divided by the total effective area yields

$$\eta_{min} = \frac{P_0}{(P_i)(A_{eff})} \qquad (3.2)$$

where

η_{min} = PANSAT's minimum solar cell efficiency,

P_0 = power generated by solar array (W),

A_{eff} = effective surface area = 1145 cm^2, and

p_i = solar constant = 1353 W/m^2.

The total power, P_0, that must be generated by the solar array is calculated by converting the orbital average power of 12.8 watts, from PANSAT's power budget, to the 58 minute sunlight period per orbit available for power generation

$$P_0 = (12.8\frac{W}{orbit})(\frac{94min}{58min}) = 20.7\frac{W}{orbit} \qquad (3.3)$$

Substituting this value into Equation 3.2 and solving for η_{min}

$$\eta_{min} = \frac{20.7}{(.1145)(1353)} = 0.134 \qquad (3.4)$$

Therefore, the minimum efficiency for PANSAT's solar cells is 13.4% under ideal, one AMO at 28°C, conditions. Conventional and hybrid solar cells have efficiencies less than this value and are not suitable.

Both black and field solar cells are of sufficient efficiency to meet PANSAT's power budget. Although a field cell is slightly less efficient than a black cell, it costs approximately 10% less and operates at lower temperature. Field solar cells are selected for the PANSAT's solar array since cost is of greater importance than efficiency in the EPS design criteria. The Spectrolab K6700 field cell, with cover slide and adhesive, is a suitable selection for PANSAT's solar cells. This type of cell is produced under various names by different manufacturers and is described below along with the selected cell cover and adhesive.

1. K6700 Solar Cell

The K6700 solar cell is a shallow diffused cell with a back-surface field and a back-surface reflector for trapping photons. The cell has a polished front surface and a multilayered anti-reflective coating of titanium and aluminum oxide. [Ref. 27:p. 1]

Table 6 lists the bare cell parameters of the K6700 cell for both 8 and 10 mil. Because transmission losses are zero across the selected cover and adhesive, the bare cell data is also the covered cell parameters. The 10 mil K6700 solar cell is selected for PANSAT because of its higher efficiency. Less damage from electron irradiation will occur because the cell is less than 30 mm. Solar cells thinner than this value cannot absorb long-wavelength light completely, where electron damage manifests itself. [Ref. 14:p. 338]

The purpose of the dual antireflective coating is to help minimize reflection losses. The dual coating is more efficient than older types of solar cells with a single coating. The titanium and aluminum coatings have a high refraction index with less absorption in the shorter-wavelengths where the K6700 cells operate.

TABLE 6. K6700 BARE CELL PARAMETERS

PARAMETER (1 AM0 @ 28°C)	DIMENSION		UNIT
	8 MIL	10 MIL	
Open circuit voltage (V_{oc})	595	595	mV
Short circuit current (I_{sc})	343	346	mA
Optimum bias voltage (V_{mp})	485	485	mV
Optimum bias current (I_{mp})	319	322	mA
Base Resistivity	10.0	10.0	Ohm-cm
Conversion efficiency	14.1	14.3	%
Max power output	154.7	156.2	mW
Cell area	2 x 4	2 x 4	cm^2
Cell thickness	0.203	0.254	mm
Cell weight	0.424	0.528	gm
Power/unit weight	364.9	295.8	mW/g
Power/unit area	19.34	19.53	mW/cm^2

2. Cell Cover

Micrometeoroids and space debris can collide with PANSAT and cause severe damage to the solar array panels. The loss of one or several of the parallel solar panels will not destroy the power generating capability of the EPS but it will limit satellite operations. Therefore, the solar cell covers should be of sufficient thickness to reduce the probability of damage. The cell cover also reduces radiation degradation to the solar cell.

The difference between micrometeoroids and space debris is their average particle density and kinetic energy.

Micrometeoroids have an average particle density 0.5 gm/cm^3 and velocity of 20 km/sec. Space debris has a higher average density of 2.7 gm/cm^3 but velocity, 10 km/sec. Micrometeoroids pose more of a threat to PANSAT's solar panels because of their higher kinetic energy. A 6 mil ceria-doped microsheet (CMX) cover on a K6700 solar cell will protect the cell from micrometeoroid damage. [Ref. 28:p. 5-24]

A CMX cover prevents discoloration of the glass from exposure to ultraviolet and charged-particle radiation. The cost of a CMX cover is less than that of a fused silica cover. [Ref. 26:p. 7-2.3]

3. Cell/Cover Adhesive

The manufacturer-recommended adhesive for bonding a CMX cover to a K6700 cell is Dow Corning 93-500 adhesive (DC 93-500). If the DC 93-500 bonding agent is used with the CMX cover, there will be no transmission losses through the solar cell cover. [Ref. 29]

4. Substrate

A preliminary design of PANSAT's substrate, for each solar panel consists of: an aluminum panel (0.30 mm thick) an epoxy/glass insulating layer (0.20 mm thick) and a 0.07 mm layer of RTV-118 adhesive to bond the substrate and solar cells together.

The panel substrate are 18.4 x 18.4 cm^2 and are made of 2014.T6 sheet aluminum [Ref 16:p. 245]. The 17 solar panel

substrates are not satellite load-bearing surfaces or structural members. However, they must be thick enough to withstand launch loads without flexing or warping to prevent damage to the solar cell interconnections.

The trade name for the epoxy/glass insulator is Kapton, manufactured by the DuPont company. It is a flame-resistant, thermal insulator and is used extensively for spacecraft thermal control. Thicknesses of 0.10 mm are common for insulating solar cells from the metal substrate, however, a typical metal substrate is made of thicker honeycomb aluminum and not sheet aluminum. The Kapton layer was increased to 0.20 mm to help reduce the heat transfer through the thin sheet aluminum.

The adhesive, General Electric RTV-118, for bonding the aluminum, Kapton, and solar cells together is a methyl-phenyl compound with superior low temperature properties. [Ref 26:p. 7.2-1]

D. ARRAY AND SINGLE CELL POWER OUTPUT AT BOL

The power output of a single solar cell and the solar array at BOL, using the K6700 series cell, is calculated as follows:

1. Single Cell Power Output At BOL

The glassed, degraded, maximum power output, P_c, of a single solar cell is defined as [Ref. 26:p. 8.6-1]

where

$$P_{C(BOL)} = (P_o)(s')(F_{T(op)})(F_M)(F_{SH})(F_{BD})(F_{CONF}) \quad (3.5)$$

P_o = initial bare cell output at one AM0 and at 28°C,

S' = effective solar intensity, including cell cover losses, solar distance and non-normal degradation factor,

$F_{T(op)}$ = operating temperature degradation factor,

F_M = miscellaneous assembly and degradation factors,

F_{SH} = shadowing factor,

F_{BD} = blocking diode and wiring loss factor prorated for a single cell, and

F_{CONF} = configuration factor.

Using the data from Table 6, the above variables for PANSAT are calculated as follows:

- P_o = 0.1562 W (from Table 6)
- Effective solar intensity, S', is calculated using the equation [Ref. 26:p. 9.4-5],

$$S' = \left(\frac{S}{D^2}\right) F_\tau \cos\Gamma \quad (3.6)$$

where

S = solar intensity,

D = array sun distance,

F_τ = solar cell cover factor, and

Γ = angle of incidence.

For the lowest level of illumination (S/D^2) is further defined as

$$(S/D^2) = \frac{S_{summer\ soltice}}{S_{mean}} = \frac{1309 W/m^2}{1353 W/m^2} = 0.967 \qquad (3.7)$$

The solar cell cover factor for a K6700 cell using a CMX cover and DC 93-500 adhesive is 1.0, indicating that there are no transmission losses through the cover and adhesive. Since the calculated effective surface area for PANSAT is already corrected for angle of incidence, Γ will be 0° for normal incidence.

Substituting and solving for S' yields

$$S' = (0.967)(1.0)\cos 0° = 0.967 \qquad (3.8)$$

- The temperature degradation factor, $F_{T(op)}$, is defined by [Ref. 26:p. 8.6-1]

$$F_{T(op)} = \frac{P_{MPT(op)}}{P_{MP}} \qquad (3.9)$$

where

$P_{MPT(op)}$ = the cell's power output at operating temperature, and

P_{MP} = the cell's power output at 1 AM0 and 28°C.

To determine the cell's power output at its operating temperature, the operating temperature is first calculated from [Ref. 26:p. 9.6-16]

$$T_{op} = \left(\frac{\bar{\alpha}_{Se}}{\bar{\epsilon}_{HF}+\epsilon_{HB}} \frac{S\cos\Gamma}{\sigma}\right)^{1/4} \quad (3.10)$$

where

$\bar{\alpha}_{Se}$ = effective solar absorptance,

S = value of the solar constant = 1353 W/m^2,

Γ = the angle between the solar cell array normal and the array-sun line,

$\bar{\epsilon}_{HF}$ = effective hemispherical front side emittance,

ϵ_{HB} = hemispherical back side emittance, and

σ = Stefan-Boltzmann constant.

For a K6700 solar cell $\bar{\alpha}_{Se}$ = 0.76, $\bar{\epsilon}_{HF}$ = 0.81, and ϵ_{HB} = 0.85 [Ref. 27:p. 7]. For PANSAT, as previously mentioned, $\Gamma = 0°$. Substituting the above values into Equation 3.9

$$T_{op} = \left(\frac{0.76}{0.81 + 0.85}\right)\left(\frac{1353 \cos 0°}{5.67 \times 10^{-8}}\right)^{1/4} = 323.3°k \quad (3.11)$$

$$T_{op} = 323.3°k - 273°k = 50.3°C$$

$P_{MPT(op)}$ can further be defined as [Ref. 26:p. 12.1-2]

$$P_{MPT(op)} = P_{MP}\left(\frac{V_{MP} + \Delta V_2}{V^{MP}}\right) \quad (3.12)$$

where ΔV_2 is the maximum power voltage shift between the operating temperature and the initial reference temperature. The voltage shift is calculated by

$$\Delta V_2 = \beta_v (T_{op} - T_{REF}) \quad (3.13)$$

where

T_{op} = 50.3°C,

T_{REF} = 28.0°C, and

β_v = temperature coefficient for voltage (V/°C).

The voltage temperature coefficient, β_v, for a K6700 cell is -0.002 [Ref. 27:p. 27]. Substituting these values into Equation 3.10

$$\Delta V_2 = -0.002(50.3 - 28.0) \tag{3.14}$$

$$\Delta V_2 = -0.045 \text{ V/°C}$$

Substituting ΔV_2 back into Equation 3.11, along with V_{MP} and P_{MP} yields

$$P_{MPT(op)} = 0.1562 \left(\frac{0.485 - 0.045}{0.485}\right) \tag{3.15}$$

$$P_{MPT(op)} = 0.1417 \text{ W}$$

Finally, substituting this value into Equation 3.9 produces

$$F_{T(op)} = \frac{0.1417}{0.1562} = 0.91 \tag{3.16}$$

- The cover assembly and degradation factor, F_M, was not addressed in Equation 3.1 and includes losses due to welding, interconnectors, and changes in resistance. For most array designs F_M will range from 0.95 to 1.00 [Ref. 26:p. 8.6-1]. A value of 0.99 for F_M is selected for PANSAT because of the array's size and simplicity.

• The shadowing factor, F_{SH}, accounts for a reduction of the solar illumination on a solar array due to blocking of the sunlight by a shadow-casting object [Ref. 26:p. 9.5-1]. The only shadow-casting objects on the PANSAT are the four whip antennas for communications. These antennas are small in diameter and will cast an insignificant shadow. Therefore, F_{SH} is assumed to be 1.0.

• The blocking and wiring loss factor, F_{BD}, for a single cell is defined as [Ref. 26:p 8.6-2]

$$F_{BD} = 1 - \frac{V_D + V_W}{V_B + V_D + V_W} \qquad (3.17)$$

where

V_D = diode voltage drop,

V_W = voltage drop of the wiring between the array and the load, and

V_B = array bus voltage at the satellite load.

There are two shottky diode drops between the solar array and load with each one being less than 0.4 volts. The wiring losses, based on PANSAT's small size, should be small with an assumed value of 0.2 volts. Since PANSAT's bus is unregulated, the voltage at the load is actually the array voltage minus the voltage drops in diodes and wiring. The bus voltage, V_{BUS}, is assumed to be the voltage of a K6700 cell at its maximum power output, 0.485 volts, multiplied by the 32

cells in series on each panel. Substituting the above values into Equation 3.8

$$F_{BD} = 1 - \frac{0.4 + 0.4 + 0.2}{(0.485)(32)} = 0.94 \qquad (3.18)$$

- The configuration ratio or aspect ratio, F_{CONF}, is 1.0 for a flat array. PANSAT is assumed to have a F_{CONF} of 1.0, despite its polyhedron shape, because each individual panel is flat. Substituting the calculated values for P_o, S', $F_{T(op)}$, F_M, F_{SH}, F_{BD}, and F_{CONF} into Equation 3.5

$$P_{C(BOL)} = (.156)(.967)(.91)(.99)(1.0)(.94)(1.0) \qquad (3.19)$$

$$P_{C(BOL)} = 0.128W$$

Therefore, a single solar cell at the beginning of PANSAT's mission will generate 0.128 watts of power.

2. Solar Array Power Output at BOL

The average power, P_{BOL}, at BOL is

$$P_{BOL} = P_{C(BOL)}\left(\frac{A_{EFF}}{A_C}\right) \qquad (3.20)$$

where

A_{EFF} = 1145 cm^2, and

A_C = cell area = 2 x 4 cm^2.

Substituting and solving for P_{BOL}

$$P_{BOL} = 0.128\ \left(\frac{1145}{8}\right) = 18.3\ W \qquad (3.21)$$

This value will satisfy PANSAT's power budget and could possibly be greater since the values for effective surface area solar illumination and operating temperatures are worst-case situations.

E. RADIATION DEGRADATION

Solar cells degrade over a satellite's mission because of irradiation from electrons and protons. A solar array's degradation in a LEO orbit is from electrons and protons in the earth's radiation belt which are trapped by the geomagnetic field [Ref. 26:p. 9-11.2]. Radiation enters the solar cell through two directions, the coverglass and the substrate. Radiation affects both the current and voltage output of the array.

Radiation damage is calculated using a normalized coefficient which is determined from a 1-MeV fluence scale. The 1-MeV fluence is used as a standard radiation environment for comparing actual damage to a solar cell from protons and electrons of various energies. The unit of fluence is 1-MeV electrons per cm^2. [Ref. 26:p. 2.5-2]

The radiation penetrating a solar cell depends on the front and back shield thickness; the front being the cell cover and the substrate being the back shield. Determining shield thickness means calculating, individually, the sum of the thicknesses in the front and back elements. The values are used to determine the total 1-MeV fluence. The 1-MeV

fluence, in turn, is compared to a solar cell's output at maximum power under various levels of radiation. The solar cell's normalized output for the computed equivalent 1 MeV fluence is the degradation factor. [Ref. 14:p. 335]

1. Shielding Thickness

Tables 7 and 8 list the shielding thicknesses for the front shield and the back shield, respectively. Also listed are the fused silica-equivalent shield thicknesses for each material. [Ref. 26:p. 8.3-2]

TABLE 7. FRONT SHIELD THICKNESS

Material	Density (g/cm^3)	Actual Thickness (mm)	Fused Silica-Equivalent Shielding Thickness (mm)
Ceria-Doped Microsheet	2.51	0.15	0.171
DC 35-900	1.08	0.1	0.5
TOTAL	-	-	0.67

TABLE 8. BACK SHIELD THICKNESS

Material	Density (g/cm^3)	Actual Thickness (mm)	Fused Silica-Equivalent Shielding Thickness (mm)
Thermal paint	1.55	0.043	0.03
Aluminum panel (2014-T6)	2.80	0.3	0.38
Epoxy/Glass (Kapton)	1.87	0.20	0.17
RTV 118	1.04	0.07	0.03
TOTAL	-	-	0.61

The total front shield thickness, from Table 7, is 0.67 mm and the rear shield thickness is 0.61 mm.

2. Determination of 1-MeV Fluence

The front and back shielding thicknesses are used separately to determine their respective 1-MeV fluence values. These fluence values are then summed together for the total 1-MeV fluence. The determination of the fluence values for the maximum power output on the solar array, P_{MP}, and the voltage at the maximum power output, V_{MP}, are sufficient for a preliminary design.

Table 9 shows the 1-MeV fluence for geomagnetically-trapped protons and electrons on a satellite in a 480 km orbit and an inclination of 30° with a front shield thickness of 0.67 mm and a back shield thickness of 0.61 mm. In PANSAT's two year mission, the 1-MeV fluence is 3.24×10^{12} e/cm^2 on the

TABLE 9. PANSAT 1-MEV FLUENCE

PARTICLES	1-MeV Flux 480 km 30^0 (e/cm^2 yr)		Mission 1-MeV Fluence (e/cm^2)	
	Front	Back	Front	Back
Trapped Electrons	4.49E+9	4.88E+9	8.98E+9	9.77E+9
Trapped Protons	1.62E+12	1.66E+12	3.24E+12	3.31E+12
Subtotal	1.62E+12	1.66E+12	3.24E+12	3.31E+12
TOTAL	(Front + Back)			6.55E+12

front shield and 3.31 x 10^{12} e/cm^2 on the back shield. The total 1-MeV fluence for computing radiation degradation is 6.55 x 10^{12} e/cm^2. [Ref. 30:p. 6-28]

3. Radiation Degradation Factor

Using the total 1-MeV fluence value computed in the previous section, the degradation factors were determined from radiation graphs for a K6700 10 mil solar cells. Table 10 lists the radiation degradation factors. The factors are high because of the relatively benign radiation environment of a low earth orbit.

TABLE 10. DEGRADATION FACTOR

Parameter	Reference	Normalized Parameter
$I_{SC\phi}$	Ref. 27: p. 48	0.98 I_{SC}
$I_{MP\phi}$	Ref. 27: p. 49	0.99 I_{MP}
$V_{MP\phi}$	Ref. 27: p. 50	0.97 V_{MP}
$V_{OC\phi}$	Ref. 27: p. 51	0.95 V_{OC}

F. LOWEST PANEL VOLTAGE AT BOL

The lowest panel voltage is determined from the lowest cell voltage, V_{MP}, at maximum power output. The lowest V_{MP} occurs at equinox which is the highest operating temperature for the solar array [Ref. 26:p. 12.2-3]. The solar cell's voltage at equinox is calculated by [Ref. 26:p. 8.7-1]

$$V_{MP} = V_{MP\phi} + \Delta V_{s/} + \beta(T_{OP} - T_{REF}) - V_2 \qquad (3.22)$$

where

$V_{MP\phi}$ = 0.97 V_{MP} (From Table 3-5),

$\Delta V_{s'}$ = K log (s'/s),

β = -0.002,

T_{OP} = 50.3°C (From Equation 3.10), and

T_{REF} = 28.0°C.

For $\Delta V_{s'}$, the value of k is the percentage of illumination lost in transmission through the cell cover. A K6700 cell with a CMX cover and DC 93-500 adhesive has virtually no transmission losses. Therefore, $\Delta V_{s'}$ is zero. Substituting and solving Equation 3.20

$$V_{MP(EOL)} = 0.97(0.485) - 0 - 0.002(50.3-28.0) \quad (3.23)$$

$$V_{MP(EOL)} = 0.426 \text{ volts}$$

This value is the lowest voltage a K6700 solar cell should generate during PANSAT's two year mission.

The minimum panel voltage is calculated from

$$V_{P(EOL)} = 32V_{MP(EOL)} - V_D \quad (3.24)$$

Substituting and solving,

$$V_{P(EOL)} = 32(0.426) - 0.3 \quad (3.25)$$

$$V_{P(EOL)} = 13.3 \text{ V}$$

The solar array will provide, at EOL, 13.3 volts to the BCR circuit and, taking into account a second diode voltage drop, a distribution bus voltage of 13.0 volts. This value is

sufficiently high enough to charge the batteries and provide unregulated voltage for operation of the communications package.

G. ARRAY AND SINGLE CELL POWER OUTPUT AT EOL

The power output, at summer solstice, of a single cell at EOL is defined as

$$P_{C(EOL)} = (P_o)(s')(F_{T(OP)})(F_M)(F_{SH})(F_{BD})(F_{CONF})(F_{RAD}) \quad (3.26)$$

where F_{RAD} = radiation degradation factor.

The other values are the same as for Equation 3.4. The radiation degradation factor is further defined as

$$F_{RAD} = \frac{P_{MP\phi}}{P_{MP}} \quad (3.27)$$

where

$P_{MP\phi} = V_{MP\phi}\ I_{MP\phi}$ (From Table 3-5), and

$P_{MP} = P_o$.

From Table 3-5, $P_{MP\phi}$ is 0.150 watts. Substituting this value into Equation 3.1

$$F_{RAD} = \frac{0.150}{0.156} = 0.96 \quad (3.28)$$

Using 0.96 for F_{RAD} and solving Equation 3.25, the power output for a single solar cell at EOL is

$$P_{C(EOL)}=(.156)(.967)(.91)(.99)(1)(.94)(1)(.96) \quad (3.29)$$

$$P_{C(EOL)} = 0.123 \text{ w}$$

1. Solar Array Output at BOL

The average power, P_{EOL}, at EOL is

$$P_{EOL} = P_{C(EOL)} \left(\frac{A_{EFF}}{A_C}\right) \quad (3.30)$$

Substituting and solving,

$$P_{EOL} = 0.123\left(\frac{1145}{8}\right) = 17.6 \text{ w} \quad (3.31)$$

This value is slightly less than PANSAT's power budget but reflects worst case conditions. The temperature at summer solstice should actually be about 10°C less which will allow the solar array to generate more power.

H. BLOCKING DIODES

Each of the 17 panels comprising PANSAT's solar array is connected to the satellite's distribution bus via a blocking diode. The blocking diode, or isolation diode, conserves energy on solar cells of panels which are nonilluminated or when the output of the string of 32 cells in series falls below the bus voltage of the satellite. Unfortunately, the

blocking diode. Blocking diodes are generally conventional, high-reliability rectifier diodes with current ratings that have been adjusted to account for limited amounts of conduction and radiation in the space environment. Higher diode operating temperatures result in lower forward voltage drops. Blocking diode design requirements are:

- Lowest possible forward voltage drop at the nominal current level and the actual diode operating temperature.
- Capability to withstand cyclic temperatures throughout PANSAT's mission life without failure.
- The preferred failure mode for PANSAT's blocking diodes is "open-circuit" so that reliability can be obtained using parallel-redundant diodes.
- The diode should have a peak-inverse voltage rating based on worst-case temperature, highest bus voltage and transient voltage spikes.

To minimize single point failure on the array/satellite interface, each blocking diode should be wired into the primary bus separately to prevent a single wire failure from isolating the solar array. PANSAT's blocking diodes can be mounted in the satellite's interior or the inside surface of the solar array panel. [Ref. 28:p. 5.5-3]

A suitable blocking diode for the PANSAT is a 1N5825 schottky-barrier rectifier approved by the Naval Research Laboratory (NRL) for space applications [Appendix D of Ref. 31]. This diode is rated at 5 amps with a dc blocking voltage of 40 volts. The 1N5825 has a maximum instantaneous forward voltage drop of 0.36, worst case, and a maximum ambient temperature of 65°C. The blocking diode's forward voltage drop, using Figure 7 and an assumed satellite interior temperature of 25°C, is estimated to be 0.27 volts. The 1N5825 is available in a high reliability package, the MBR5825H1. A MBR5825H1 is screened for high temperature storage, temperature cycling, constant acceleration and hermetic sealing. Additionally, the devices are processed through a high temperature reverse bias and a 24 hour forward burn-in period. [Ref. 32:p. 3-55].

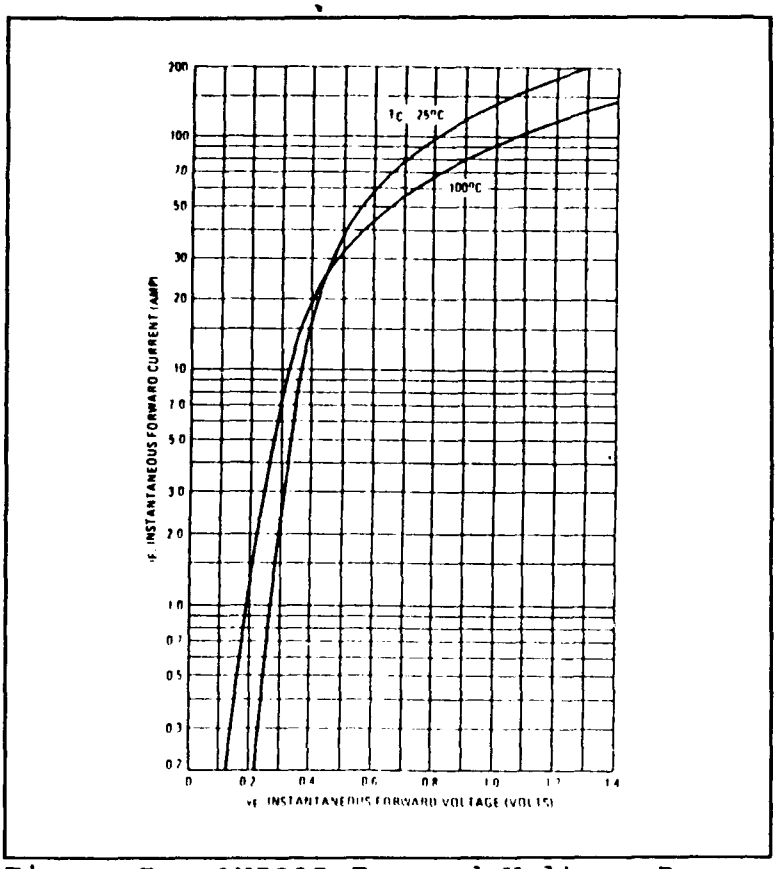

Figure 7. 1N5825 Forward Voltage Drop [From Ref. 32]

IV. BATTERY SELECTION AND CONFIGURATION

A. CONSIDERATIONS

Spacecraft using solar arrays as primary power sources require a means of storing the power for use during eclipse or when the load demands exceed the output of the solar array. Currently spacecraft use rechargeable, or secondary, cells for storing electric power generated by the array. Secondary cells utilize chemical reactions to generate current and are capable of being recharged many times by applying current to the cell, thereby reversing the chemical reaction. Considerations in proper battery selection and sizing are battery voltage, capacity, application, charge/discharge characteristics and life expectancy.

1. Battery Voltage

A distinction must be made between cells and batteries. A cell is the basic electrochemical building block of batteries which consist of one or more cells. The battery voltage depends on the number of cells connected in series and the electrochemistry of the cell which, in turn, determines cell voltage. The required capacity is achieved by connecting two or more identical batteries in parallel. Different types of secondary cells produce different voltages which increase

or decrease the number of cells required for a given battery voltage. [Ref. 33:p. 11]

2. Capacity

While cell voltage is determined by its chemistry, the cell capacity is a variable quantity dependent on application, rate of discharge, and cell volume. Cells of the same type construction but different capacities generally have similar charge and discharge characteristics scaled by the cell's capacity. The nominal or typical capacity of a cell is expressed as its **C** rating. The **C** rate defines the current flow rate (ampere-hour) which is numerically equal to the cell's capacity. In conjunction with examining a cell's **C** rating, the design process requires a determination of a cell's ability to supply the required number of watt-hours. The watt-hours are determined by the cell capacity and the cell voltage. [Ref. 33:p. 13]

3. Charge/Discharge Characteristics

When a depleted cell is charged, the cell voltage rises above the nominal discharge voltage of the cell. As the cell approaches full charge, the voltage rise increases rapidly. Overcharging in most cells produces excess heat and can cause irreversible cell damage. Charge rate and ambient temperature significantly affect battery charging efficiency. [Ref. 14:p. 352]

Charging normally takes place at a high current. As the cells approach full charge, the battery is switched to a slower rate, or trickle-charge, that is a fraction of the ampere-hour rating of the battery [Ref. 34:p. 112]. The trickle-charge replaces energy lost through self-discharging of the battery. PANSAT's BCR will provide battery charging every orbit, thereby eliminating the requirement for a fast and slow rate of charge. The battery charging process is not totally efficient. Temperature dependency and parasitic generation of various gases reduce charging efficiency [Ref. 33:p. 145]. The power budget allows one watt for BCR charging inefficiencies, which is based on an assumed charging efficiency of 90%.

The cell discharge characteristics which describe the cell's performance are capacity and voltage. A desirable characteristic is for the cell voltage to remain relatively constant until almost all of the rated capacity is discharged. Figure 10 depicts a typical cell discharge curve. At the end of the discharge period the voltage drops off sharply. The mid-point voltage on Figure 8 represents the voltage delivered by the cell when 50% of the cell's capacity has been discharged. The mid-point voltage is, approximately, the average value of discharge voltage for a cell. In Figure 8, ΔV represents the difference in discharge voltage for a fully charged cell and a depleted cell. The point, V_{begin} is the open

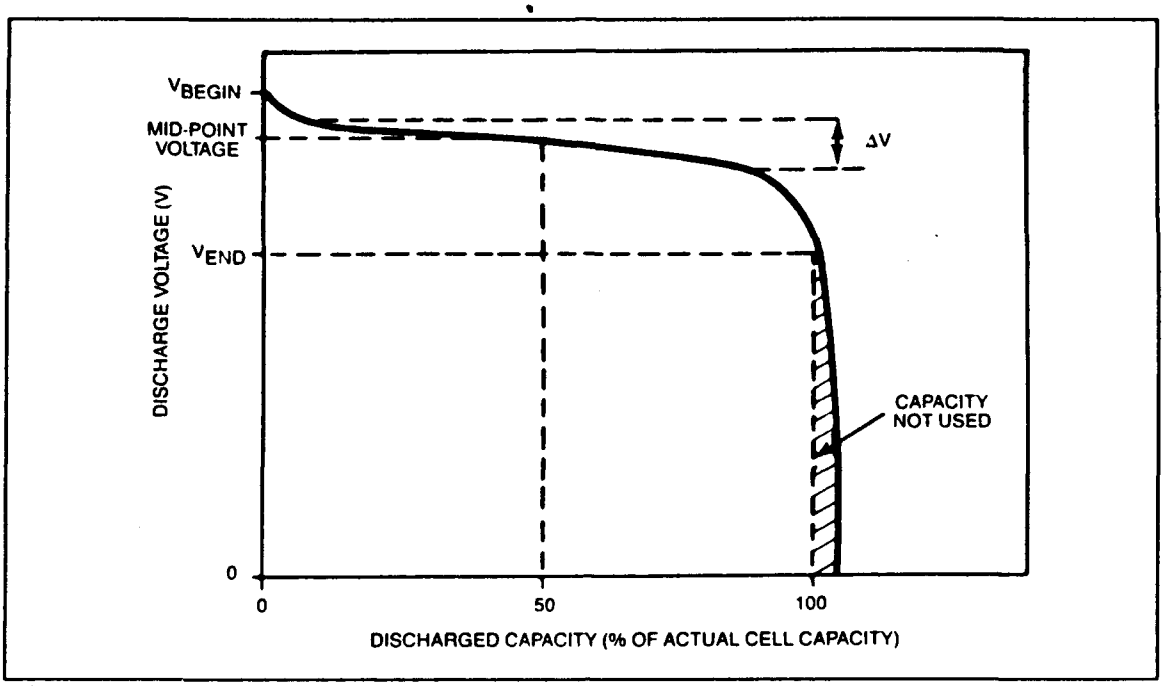

Figure 8. Typical Cell Discharge Curve [From Ref. 33]

circuit voltage for a fully charged cell and V_{end} is the discharge voltage for the depleted cell. [Ref. 33:p. 34]

Decreasing the discharge rate increases cell capacity. The cell discharge curve shape varies with cell type, the chemistry of the cell, and the slope of the voltage drop near cell depletion. Temperature and history of the cell also determine the discharge voltage characteristics. [Ref. 33:p. 52]

4. Life Expectancy

The life expectancy of a cell is directly related to its application. There are two general applications for batteries, float and cyclic. In a float application, a cell spends the majority of its life on charge as a backup power

source. By constrast, cyclic applications require the cell to be drained to a preset DOD on a regular basis. A high DOD reduces the cell's life considerably. Float applications are aimed at preserving the life of the cell by using a very shallow DOD which is replaced on a continuous or near-continuous basis. The battery charging process is related to the type of application. [Ref. 33:p. 12]

B. AEROSPACE VS. TERRESTRIAL CELLS

Table 11 lists suitable candidate cells for PANSAT's EPS. Although the devices appear to be comparable, the aerospace-rated cells, nickel-hydrogen (Ni-H_2) and nickel-cadmium (Ni-Cd), are vastly superior because of their ruggedness and high reliability. Additionally, these devices are intended for the space environment and do not require a sealed battery container. Unfortunately, cost is a prohibitive factor. Using the aerospace Ni-Cd cells listed in Table 11, PANSAT's batteries would cost approximately $50,000 which is a third of the total projected budget. The NPS SSAG has obtained surplus aerospace Ni-Cd cells, rated at 15 amp-hours, originally intended for the Global Positioning Satellite (GPS). These cells are past their storage life and, until proven otherwise, are not considered reliable for the PANSAT project.

Terrestrial cells, Ni-Cd and lead-acid (Pb-Acid), can perform the same functions in PANSAT's EPS, with a few restrictions, at a fraction of the cost. AMSAT's OSCAR series

satellites use terrestrial Ni-Cd cells exclusively and both NUSAT and GLOMR used Pb-Acid cells. Terrestrial cells are designed to operate at atmospheric pressure and require a pressurized container for a space environment. Terrestrial batteries, based on cost considerations, are selected for the PANSAT.

TABLE 11. PANSAT CANDIDATE BATTERIES

Type	Voltage (V)	Special Energy (Watt-Hr/Kg)	Cell Rating (Amp-Hr)	Operating Temp (°C)
Ni-Cd (space)	1.29	28	6.0	-10 to 35
Ni-H2 (space)	1.32	45	30.0	-25 to 35
Ni-Cd (terrestrial)	1.29	35	4.0	-25 to 40
Pb-Acid (terrestrial)	2.10	30	5.0	-40 to 60

C. TERRESTRIAL NI-CD VS. PB-ACID

The P-440DE terrestrial sealed NiCd cell manufactured by Panasonic [Ref. 35:p. 72] was compared to the Pb-Acid X-Cell manufactured by Gates Energy Products. The Panasonic NiCd was selected for comparison based on the availability of data from the manufacturer. This cell's capacity is larger than NiCd cells flown on OSCAR satellites but has similar characteristics. Gates Pb-Acid cells have been used successfully on numerous space shuttle GAS cannister

experiments. GLOMR used D-size Gates Pb-Acid cells where as NUSAT used the X-Cell. Both the NiCd and Pb-Acid cells are inexpensive. The major advantages and disadvantages of NiCd and Pb-Acid cells follow.

1. Advantages/Disadvantages of Terrestrial NiCd Cells

The advantages of a NiCd cell are [Ref. 33:p. 6]:

- Relatively low internal resistance and high, flat voltage characteristics during high current discharge.
- 500 - 2300 charge/discharge cycles when used in cyclic operations.
- Leakproof with a resealable vent in an atmospheric environment.

The disadvantages of NiCd cells are:

- A 'memory effect' for both terrestrial and space-rated Ni-Cd cells which causes a loss of capacity over extended periods of time. This can be prevented by periodic deep discharging of the batteries [Ref. 14:p. 353].
- A cell voltage, at end-of-cell life, of 1.2 volts vice 2.0 for Pb-Acid. This requires nine NiCd cells in series, vice five for Pb-Acid, to obtain a 10.0 volt battery bus.
- Ni-Cd cells do not tolerate overcharging.

- Temperatures below or above 20 - 30°C result in decreased efficiency [Ref. 35:p. 17].
- Susceptible to cell damage, more so than Pb-Acid, from varying electrical characteristics between cells in a battery.

2. Advantages/Disadvantages of Pb-ACID Cells

The advantages of Pb-Acid cells are:

- Higher ampere-hour rating for the X-Cell compared to the P-440DE NiCd.
- Extended life of eight years when used at a shallow DOD.
- Tolerates variations in temperature better than a NiCd cell.
- Sealed construction with safety vent.
- Can accept periodic intervals of overcharging without cell damage.
- Can repeatedly withstand deep discharging of 100% capacity.

The disadvantages of a Pb-Acid cell are:

- It weighs more than a comparable NiCd cell.
- The discharge curve at high current rates is not as flat as a NiCd cell.
- Severe overcharging could cause the safety vent to release potentially explosive oxygen and

hydrogen gases. This is considerably more of a problem in Pb-Acid cells than in NiCd cells.

3. PANSAT Cell Selection

The Gates Pb-Acid X-Cell is selected for PANSAT for several reasons. The primary reason is the ability of the X-Cell to tolerate overcharging. The solar array will generate more power at a colder operating temperature after the satellite exits eclipse and, until the surface of the satellite warms up, an overcharge condition can occur. If NiCd cells are used, the solar array's output must be maintained at a single point on the solar array's power curve to prevent overcharging of the cells from power fluctuations. This operation, as pointed out earlier, is used by the OSCAR-series satellites and is considerably more complex. NUSAT did not use a BCR for its single battery and suffered no overcharging damage [Ref. 36]. Out-gassing from overcharging is not expected to be a problem since the batteries will be in a sealed pressurized container with venting capabilities. A second reason for selecting a Pb-Acid cell is its ability to handle wider ranges of temperatures.

The Gates D-Cell, rated at 2.5 ampere-hours, is an alternate candidate for PANSAT if weight becomes a problem. The reason the X-Cell was selected over the D-Cell was to provide the largest battery capacity possible for a 10 volt battery bus. The X-Cell has the capacity to withstand

repeated use of the transmitter over several orbits without draining the batteries.

D. GATES LEAD ACID X-CELL

The X-cell Pb-Acid cell is guaranteed by the manufacturer to generate 2.1 volts at 5 ampere-hours. The X-Cell has a mass of 0.37 kg and a diameter of 44 mm with a height, including terminals, of 8.1 mm [Ref. 37:p. 58].

Figure 9 is a plot of the duration of discharge, in hours, and the cell's output current for various Pb-Acid cells. After one hour of discharge the X-Cell generates less than 5 amps. This is not a problem since the maximum time the batteries will be required to discharge is 36 minutes in eclipse and the discharge current should only be 0.5 ampere, based on an eclipse power demand of 5.1 watts and a battery bus voltage of 10.5 volts.

The discharge characteristics for the X-Cell in eclipse are shown in Figure 10. The satellite's internal temperature is assumed to be 0°C. The discharge rate for both batteries in eclipse is 0.5C or C/10. Since there are two batteries in parallel, the individual discharge rate is one-half of this value or C/20. Figure 10 indicates that, for a C/20 rating for each cell at 0°C, the battery bus voltage and the distribution voltage should remain at or above the 10.5 volts for the 36 minutes of eclipse. Temperature, both in and out of eclipse, should not affect battery performance appreciably.

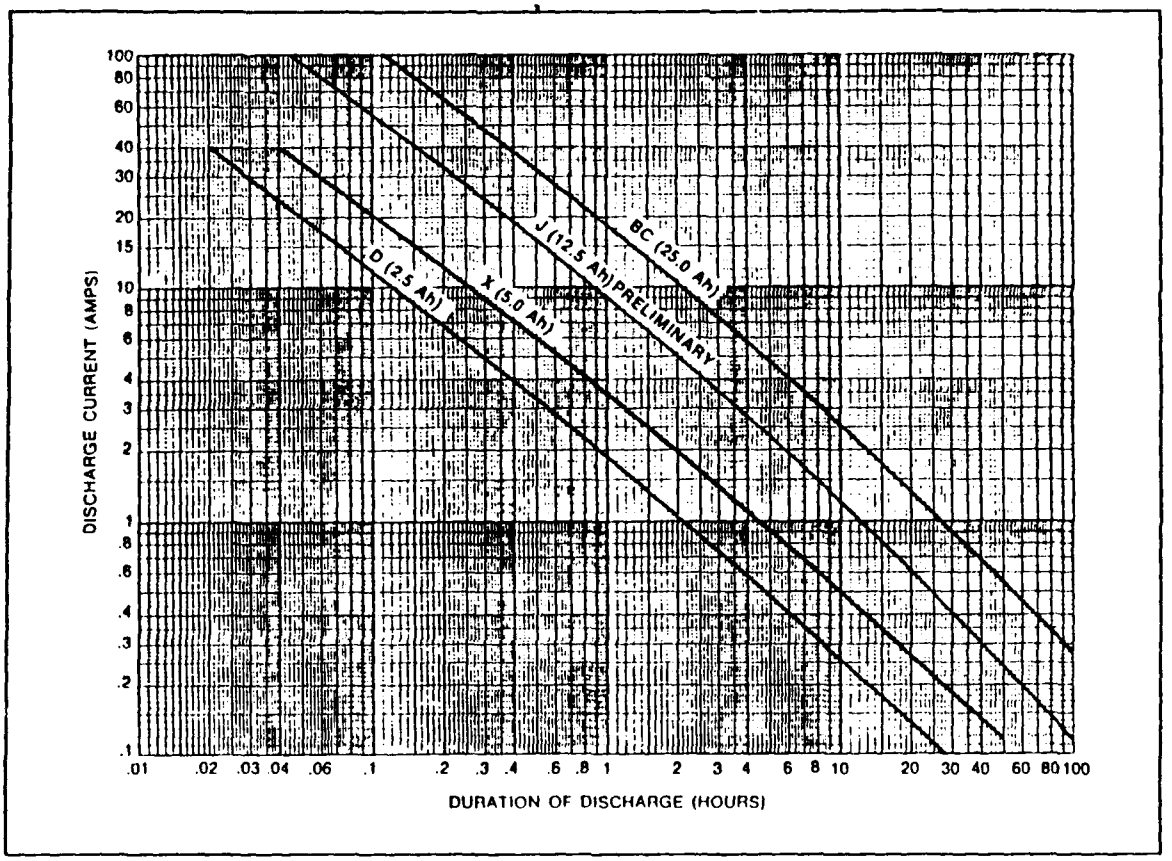

Figure 9. Discharge Current vs. Discharge Time [From Ref. 37]

The X-Cell is considered depleted when the capacity is at 20% and the open circuit voltage of the cell is 2.0 volts. PANSAT's battery bus, although designed to clamp at 10.5 volts, will continue to operate down to 10.0 volts. The BCR is designed to prevent this bus voltage from being reached. The cells should not be allowed to discharge below 1.81 volts per cell because the recharge characteristics of the cell change and longer charge times may be required [Ref. 37:p. 22].

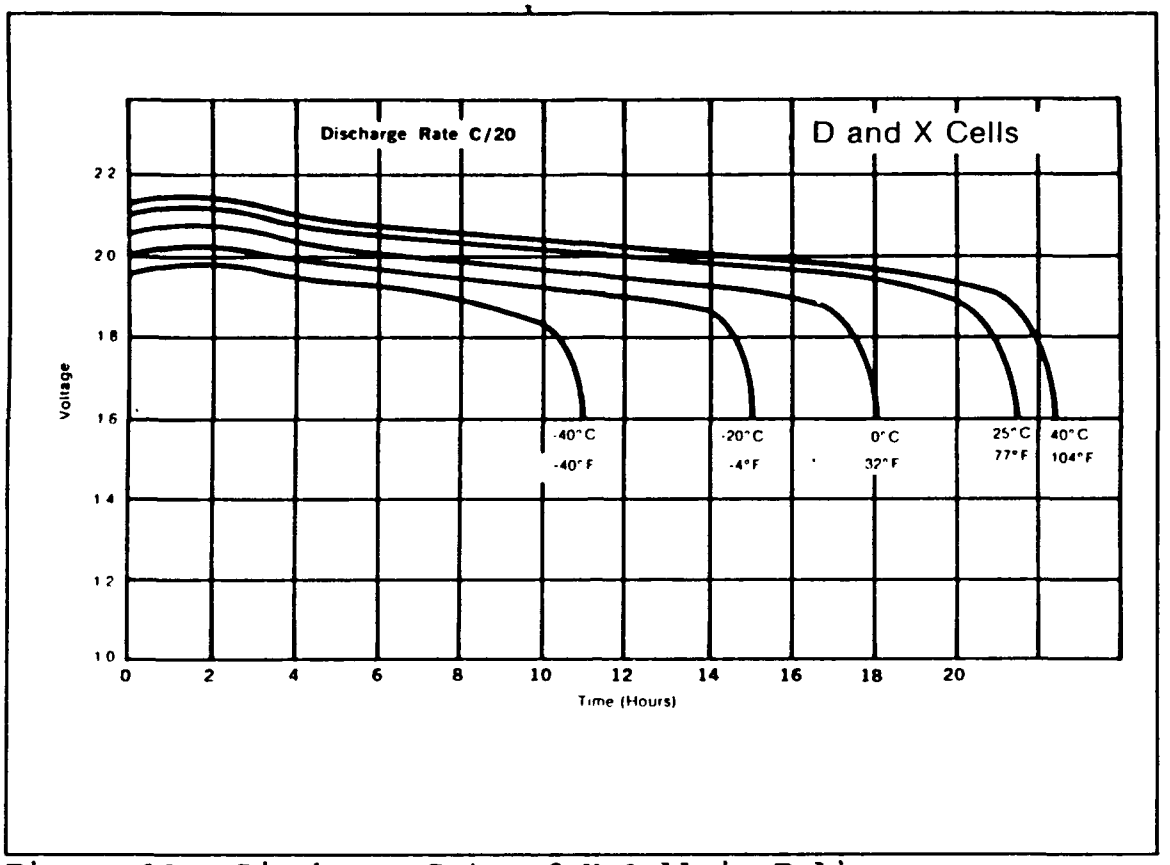

Figure 10. Discharge Rate of X-Cell in Eclipse [From Ref. 37]

PANSAT will use a float application since charging is available during each orbital period and a two-year mission would require a cyclic life in excess of the X-Cell's capabilities. Figure 11 shows the float life for a Gates Pb-Acid cell based on charging voltage per cell and temperature. PANSAT's two-year mission is well within these limits. At 20°C the expected float life of a cell is greater than eight years [Ref. 37:p. 51].

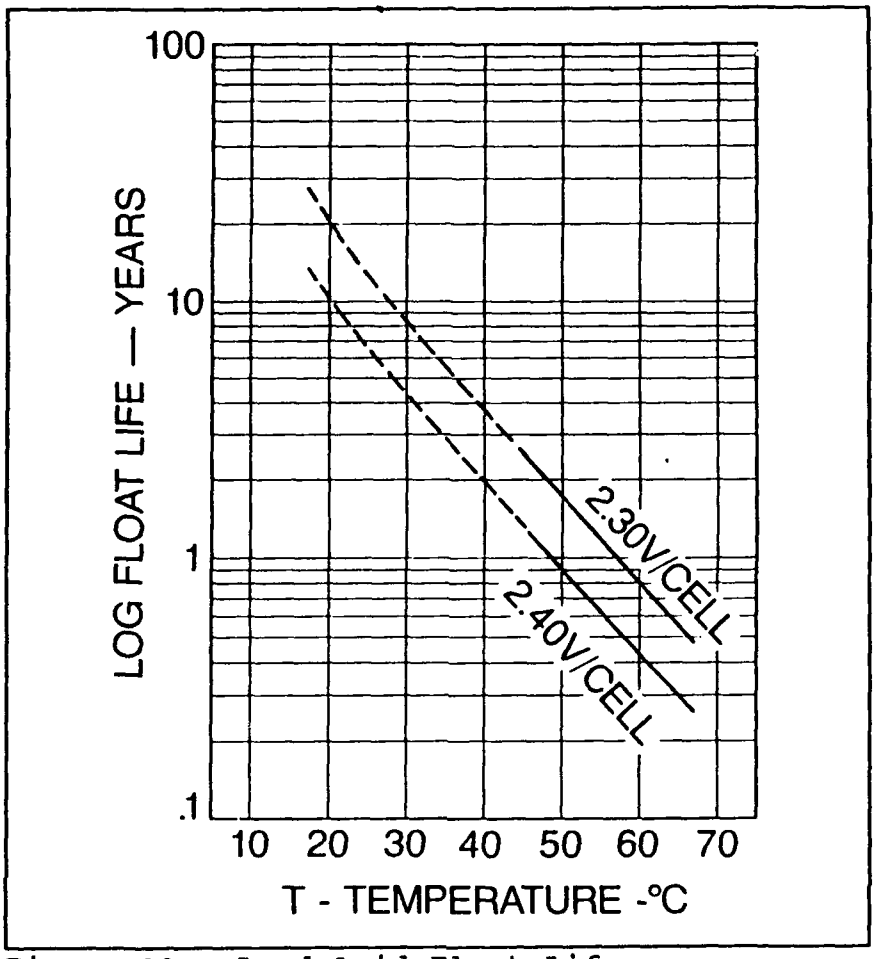

Figure 11. Lead-Acid Float Life
[From Ref. 37]

E. PANSAT BATTERY CONFIGURATION

Each PANSAT battery will consist of five 2.1 volt Gates lead-acid cells in series. Each cell's electrical characteristics should be measured and an attempt made to match the six cells, in each battery, to avoid variations in charging current. Figure 12 illustrates the configuration for a PANSAT battery. The discharge diode prevents a battery

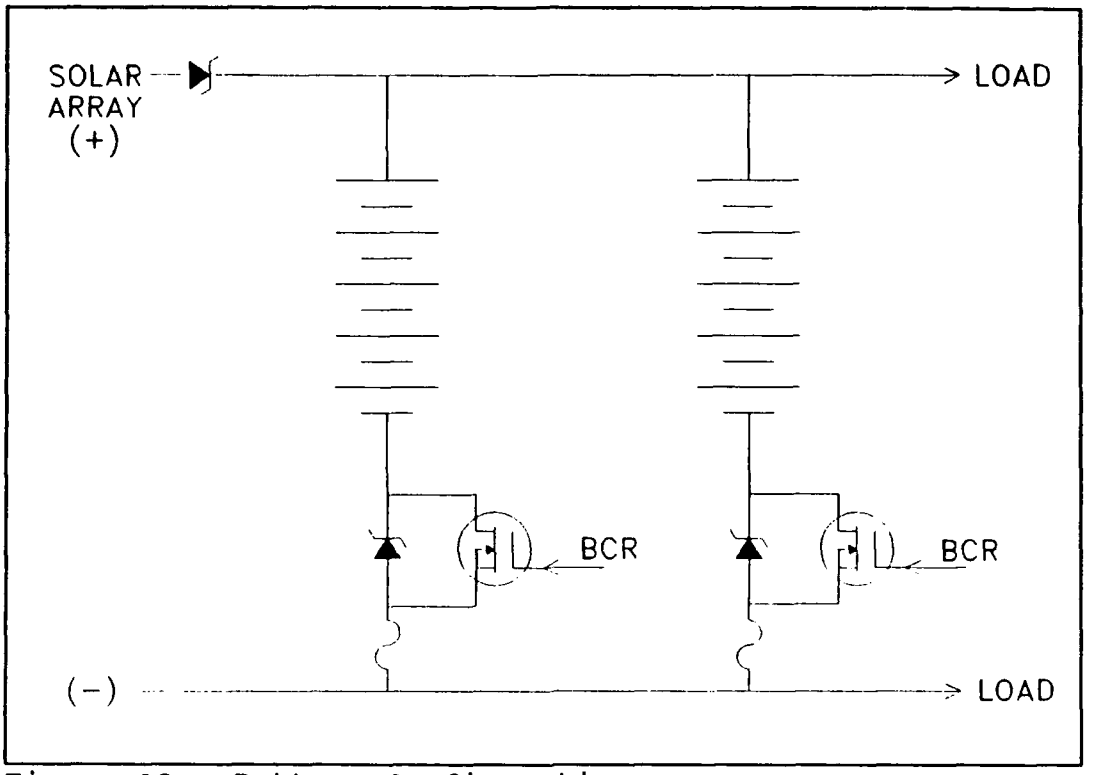

Figure 12. Battery Configuration

from being overcharged by the solar array when the battery is at full capacity. Also, if a cell shorts out in the battery and the bus voltage drops below 10.5 volts, the discharge diode of the failed battery prevents the good battery from discharging into it. A transistor switch connected across the discharge diode and, controlled by the BCR, allows the discharge diode to be bypassed for charging. Batteries in parallel normally have a charge diode which prevents a shorted cell from accepting all of the charge current. However, since the PANSAT BCR charges the batteries alternately, this condition will not occur and a charge diode is not required for each battery. [Ref. 37:p. 36]

The fuse, shown in Figure 12, represents an electrical interrupter which prevents an overcurrent condition from occurring when attempting to charge a battery with a shorted cell. Batteries must have circuit interrupters rated below the battery's short circuit current capability. Interrupters may be fuses, circuit breakers, or thermal switches. The interrupters should be in the ground leg of each battery so that battery grounds inside the battery case may be sensed and interrupted. Selection and integration of the interrupter is not considered in this thesis. [Ref. 38:p. 5]

F. PANSAT BATTERY CHARGING

There are two general methods of charging batteries [Ref. 33:p. 24]:

- constant voltage is a method of charging where the charge voltage is maintained at a fixed value and the current is varied. As the batteries approach full capacity, the current tapers to a minimum.
- constant current uses a constant current source with a varying voltage.

While both methods could be used for PANSAT's lead-acid cells, the constant voltage source is the simpler method for the EPS. A variation of the constant voltage charging process is float charging for batteries used in float applications. PANSAT's BCR will employ this method. Whenever the batteries drop below a fraction of their capacity, the BCR will alternately

begin charging the two batteries with whatever power is available from the solar array.

Figure 13 is the percent of rated capacity for a lead acid cell. The measurement of the open circuit voltage of a cell to determine the state of charge, cell capacity, is based on the relationship between the electromotive force and the specific gravity of sulfuric acid in the cell [Ref. 37:p. 21]. From Figure 13, the open circuit voltage of a cell that is at 100% capacity is approximately 2.18 voltages. Ideally, whenever PANSAT's batteries drop below 10.9 volts the BCR should begin charging the batteries. It should be noted that repeated tests, by the author, indicate the open circuit voltage of the cell remains at 2.18 volts for only 10 - 15 minutes due to self-discharge and that an open circuit voltage of 10.8 volts, for five cells, is more realistic. Therefore, 10.8 volts is selected as the set point for determining when the batteries need charging. The minimum voltage required to charge PANSAT's batteries is 11.5 volts [Ref. 37:p. 35]. A charge voltage less than this amount will be insufficient to recharge the batteries. The manufacturer recommends that float charging for a constant voltage charger should be maintained between 2.3 and 2.4 volts per cell. Continuous charging at greater than 2.4 volts per cell accelerates grid corrosion and reduces the cell's life expectancy [Ref. 37:p. 30]. This indicates that PANSAT's batteries should have a maximum charge voltage of 12.0 volts and that the distribution

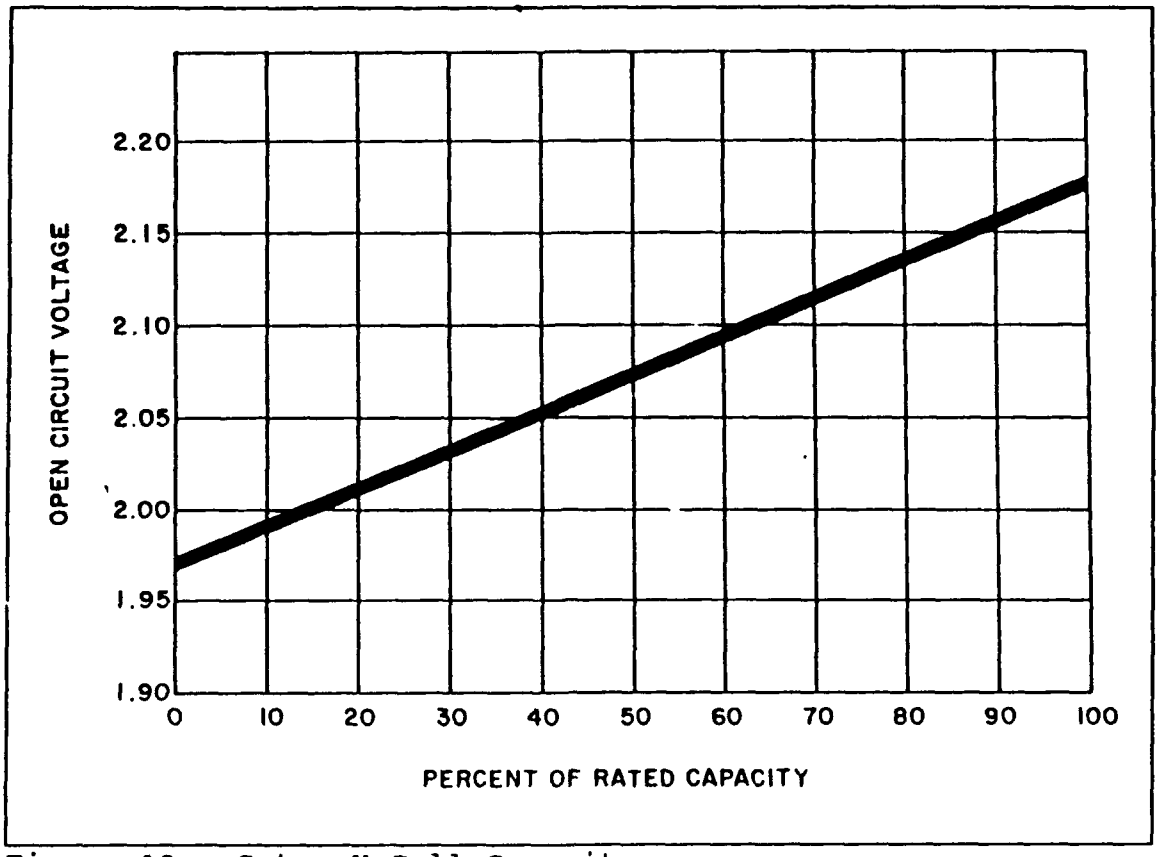

Figure 13. Gates X-Cell Capacity
[From Ref. 37]

bus voltage of 13.5 volts is too high for battery charging. However, the distribution bus voltage is an approximation that does not take into account wiring loss voltage drops. Furthermore, float charging for PANSAT's batteries is not continuous since the BCR alternates battery charging and charging is not available during eclipse. Finally, since the float-life of a Gates lead-acid cell is approximately eight years, the slight overvoltage in charging PANSAT's batteries can be tolerated.

As previously mentioned, the BCR will use the excess power generated from the solar array to charge the batteries. Assuming battery charging with the transmitter off and taking into account the other load demands of 6.6 watts, the solar array generates approximately 0.96 amps for charging. The charge rate is defined as

$$C_{charge} = \frac{\text{Charge Current}}{\text{C rate of battery}} \qquad (4.1)$$

where

Charge current = 0.96 amps, and

C Rate of battery = 5.0.

Therefore, the charge rate is approximately 0.192 C. For one orbital period the BCR can provide, operating when the transmitter is off, approximately 6.5 watt-hours, based on open circuit voltage, to the batteries. If the satellite operates the transmitter once per orbit there is a deficit of four watts for 24 minutes, since the peak load demand is 22.3 watts and the solar array can only provide 18.3 watts at BOL. Therefore, the batteries must supply 1.6 watt-hours to the transmitter per orbit. This leaves a surplus of 5.0 watt-hours available for the batteries. However, the eclipse power requirements, from Table 4, are 3.1 watt-hours leaving a total surplus of 1.9 watt-hours per orbit.

If the transmitter is used multiple times on repeated orbits and the batteries are allowed to drain down to minimum capacity, 20% at 10.0 volts, the time required to recharge the

batteries is approximately 11 hours or 12 orbits based on manufacturer provided data [Ref. 37:p. 25].

G. BATTERY CONTAINMENT

NASA requires a sealed battery box design with out-gas venting due to the possible production of explosive gases during charging [Ref. 39:p. 91]. Additionally, the manufacturer strongly recommends that lead acid cells, despite being sealed, should not be used in a non-vented container [Ref. 37:p. 53]. The battery containment box should be pressurized with nitrogen and have an aluminum core with a nonconductive electrolyte resistant internal coating. The cells require top and bottom restraint plates to prevent damage during launch loads. All plumbing parts should be high-pressure close-tolerance nitrogen stainless steel fittings with butt welds where necessary. [Ref. 40:p. 27]

The Space System Academics Group has already designed a lead-acid battery containment box for a thermoacoustic refrigerator for use in a space environment [Ref. 41:p. 13]. The container could be downsized to accommodate one or both batteries for the PANSAT. Battery mass distribution about PANSAT's center of gravity could be achieved by using two separate containers, locating one container above the mid-deck and the other below.

V. BATTERY CHARGE REGULATOR (BCR)

A. PANSAT BCR OPERATION

As PANSAT leaves eclipse, the solar array is illuminated and begins providing a nominal 13.8 volts as supply voltage, V_p, for the BCR components, activating the BCR circuit. Figure 14 is a block diagram of the BCR circuit. Comparator #1 measures a sample of battery #1's voltage, V_{B1}, and compares it to a 5 volt reference source. If V_{B1} is less than 10.8 volts, the comparator will generate a low output signal to the reset function of a master-timer, enabling or disabling it. The master-timer is configured as an astable vibrator generating a square wave pulse with a duty cycle of 48%. The output square wave opens and closes a power MOSFET connected across the distribution bus and battery #1, bypassing the battery's blocking diode. When the square wave is high, the charging MOSFET is closed and charging takes place. When the clock pulse goes low, the MOSFET opens and charging of battery #1 is inhibited by its diode. The square wave output of the master- timer is also sent to a synchronization MOSFET which synchronizes a second timer, the slave-timer.

The comparator for battery #2 measures a sample of the battery voltage, V_{B2}, and compares it to a second 5-volt reference source. If V_{B2} is less than 10.8 volts, battery #2's

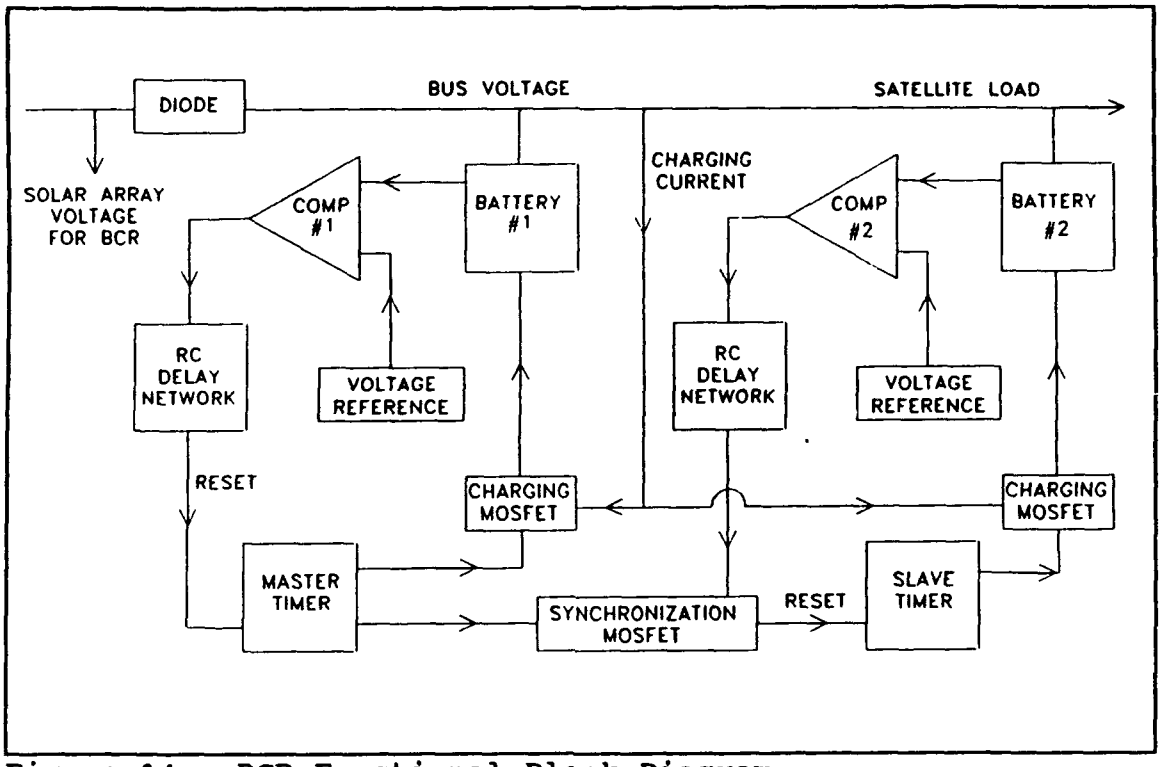

Figure 14. BCR Functional Block Diagram

voltage comparator sends a low signal to the sychronization MOSFET. This signal, along with the output of the master-timer, controls the reset function on the slave-timer, enabling or disabling the timer. The configuration of the slave-timer is identical to the master and the charging operation of the second battery is the same as the first.

Charging of either battery continues as long as each battery's comparator receives a battery voltage less than 10.8 volts referenced to its respective 5 volt source. When the battery voltage exceeds 10.8 volts, the comparator output goes high, disabling the timer, and charging ceases for that particular battery after a short delay. Ideally, both

batteries should begin and terminate charging within one charging cycle of each other.

Simultaneous charging of both batteries cannot occur because the slave-timer is controlled by the synchronization MOSFET. When the master-timer's output is high, the synchronization MOSFET closes, disabling the slave-timer. Only when the synchronization MOSFET is open and the output from comparator #2 is low can the slave-timer generate a clock pulse, closing the power MOSFET on battery #2 for charging.

An RC network between each comparator and timer serves two functions:

- The RC network prevents erroneous comparator signals from being sent to the timer when the battery voltage is high due to a charging pulse.
- A capacitor keeps the timer running an additional 9 seconds to overcharge the battery slightly above the setpoint of the comparator to prevent repeated cycling of the BCR.

B. BCR CIRCUIT REALIZATION

Figure 15 is the circuit realization of Figure 14. The components used are standard off-the-shelf CMOS devices. Table 12 lists the parts, available in military-rated packages. Manufacturer's data for each device can be found using the applicable reference in Table 12. All transistors are pure-enhancement N-channel power MOSFET's. The functional

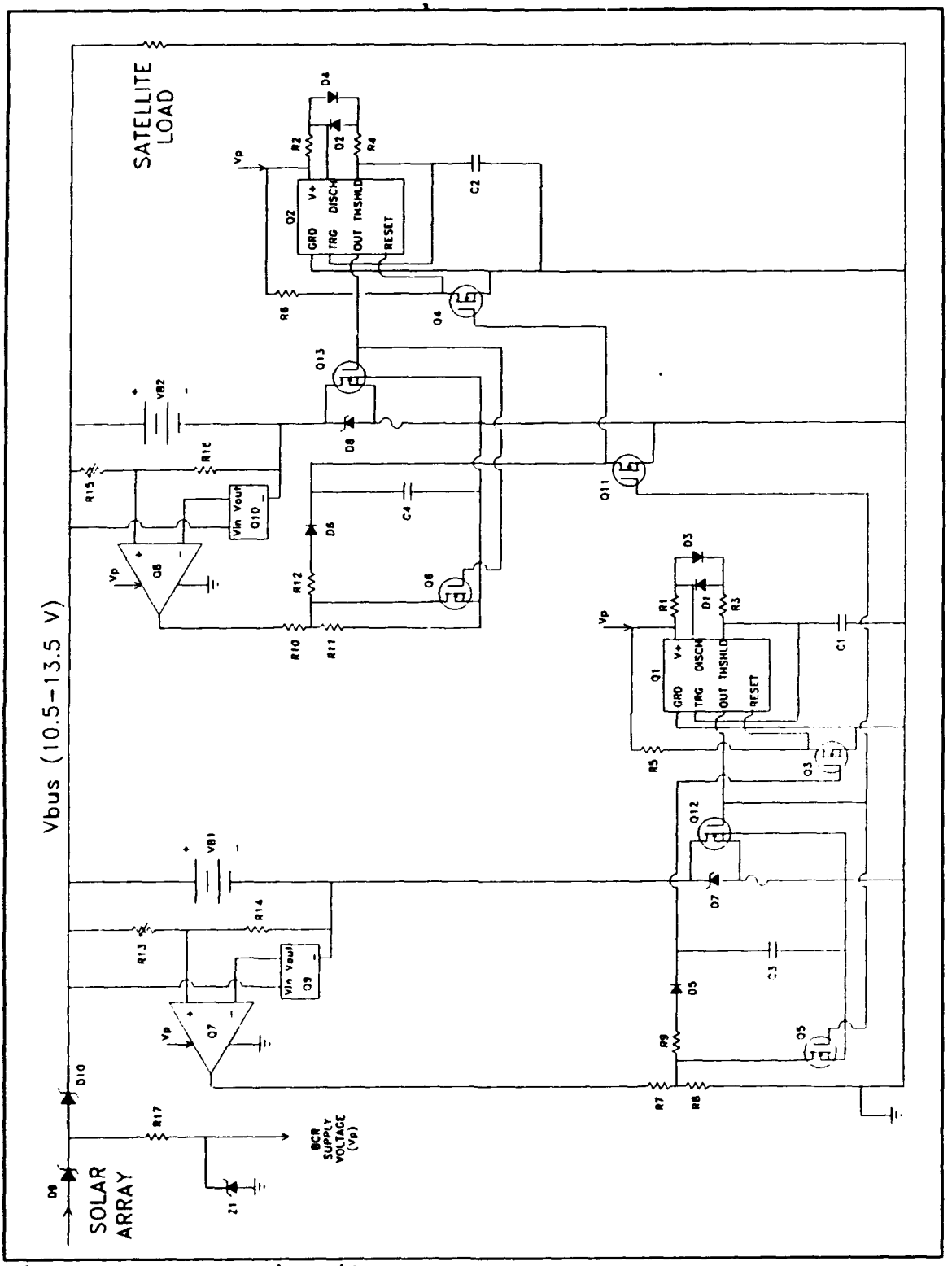

Figure 15. BCR Circuit

blocks of Figure 14 are physically realized with the following components:

1. Astable Vibrator Function

Pulse modulation of each of the power MOSFET's is performed by two MAXIM ICM7555 timers configured as astable vibrators. The configuration for the master and slave timers are identical. The ICM7555, a CMOS version of the LM555 timer, is a general multipurpose timer. Two discrete timing resistances for the master-timer, R_1 and R_3, determine the duty cycle of the circuit. A timing capacitor, C_1, in conjunction with the resistances, determine the frequency of the circuit. Charge and discharge diodes, steering diodes, are also used to control the timer's operation.

TABLE 12. BCR COMPONENTS

Component	Schematic Designation	Manufacturer's Reference
MBR5825H1	D_7, D_8, D_9, D_{10}	Ref. 32:p. 3-55
1N5355	Z_1	Ref. 32:p. 4-67
MAX673MJA	Q_9, Q_{10}	Ref. 42:p. 3-7
ICM7555MJA	Q_1, Q_2	Ref. 42:p. 8-9
LT1017M	Q_7, Q_8	Ref. 43:p. 5-37
1N914B	D_1, D_2, D_3, D_4, D_5, D_6	Ref. 44:p. 281
RFH45N05	Q_{12}, Q_{13}	Ref. 45:p. 3-344
2N6660	Q_3, Q_4, Q_5, Q_6, Q_{11}	Ref. 46:p. D-2

The BCR frequency is selected two magnitudes greater than the satellite tumbling frequency. This precludes the bus

voltage ripple, generated by the BCR frequency, from being superimposed on the ripple voltage induced by satellite rotation. The BCR frequency, F_{BCR}, is calculated as

$$F_{PM}=100\left(\frac{0.1\ \text{rad}}{\text{sec}}\right)\left(\frac{1\ \text{sec}}{2\pi\ \text{cycle}}\right) \qquad (5.1)$$

$$F_{PM}=1.60\ \text{Hz}$$

The duty cycle for both ICM7555's is 48%. The 2% dead time between pulses allows for timing errors in the circuit. The duty cycle, D, can be expressed as

$$D=\frac{R_A}{R_A+R_B} \qquad (5.2)$$

where

$D = 0.48$,

$R_A = R_1$ or R_2, and

$R_B = R_3$ or R_4.

Substituting and solving for R_A in Equation 5.2,

$$R_A = 0.923R_B \qquad (5.3)$$

To calculate R_A and R_B, the expression BCR frequency must also be solved;

$$F_{BCR} = \frac{1.46}{(R_A+R_B)C_x} \qquad (5.4)$$

where

F_{BCR} = 1.60 Hz, and

C_x = C_1 or C_2.

Selecting a reasonable capacitance for C_x of 0.47μF and substituting Equation 5.4 simplifies to:

$$R_A + R_B \approx 1.94\ M\Omega \qquad (5.5)$$

Substituting Equation 5.3 into Equation 5.5 and solving for R_A and R_B, the values of the timing components for either the master or slave ICM7555 are found to be:

R_A = R_1 or R_2 = 0.92 MΩ

R_B = R_3 or R_4 = 1.00 MΩ

C_X = C_1 or C_2 = 0.47 μF

The drain of a small MOSFET, Q_3, is connected to the supply voltage reset pin of the timer. The gate is driven by the voltage comparator via the RC delay network depicted in Figure 15. When the battery requires charging, the low signal from the voltage comparator, Q_1, keeps the gate of Q_3 open and the reset to the master-timer is held high, enabling it. After the battery is fully charged, the signal from Q_1 is delayed slightly, keeping the gate on Q_3 open and allowing the battery to continue charging. The gate closes after the delay and the reset voltage is connected to ground via the source on Q_3.

2. Voltage Comparator Function

The voltage comparator for the master-timer's battery uses the components Q_7, Q_9, R_{13}, and R_{14}. The values and the

operation of the second battery's voltage comparator are a duplicate of the master-timer's. A voltage divider, R_{13} and R_{14}, is used to reduce the nominal battery voltage from 10.8 volts to 5.0 volts. The resistor, R_{14}, is an adjustable potentiometer used to adjust the desired setpoint. The 5.0 volt reference source, Q_9, is a Maxim MAX673 precision reference device connected across the battery terminals. The MAX673 has an input, pin 3, for ambient temperature and adjusts its output to within 2 ppm/°C. [Ref. 42:p. 3-8]

A LT1017 dual CMOS voltage comparator, Q_7, compares the divided-down battery voltage against the output from Q_9. If the value is less than the reference voltage, a low signal, indicating battery charge is required, is sent to the master-timer via a RC Delay Network. If the divided-down battery voltage is higher than Q_9's output, the comparator generates a high signal to secure battery charge.

3. RC Delay Network

The RC delay networks for the master and slave timers are identical with the following exception. The output of the RC delay network in the master-timer circuit directly opens and closes the gate on the master-timer's reset transistor, Q_3. The output of the slave-timer's RC delay network, however, is connected to the drain of the synchronization MOSFET, Q_{11}, and only drives the slave-timer's reset transistor, Q_4, when the gate of Q_{11} is open.

The RC delay network for the master-timer is comprised of, from Figure 15, R_7, R_8, R_9, D_5, C_3, and Q_5. The resistors R_7 and R_8 divide the output from the voltage comparator Q_7 down to a sufficiently low value of 3.0 volts. When charging is taking place on V_{B1}, an erroneous high signal from Q_7 is sent to the master timer. However, this signal is shunted to ground by the shunt transistor, Q_5, which operates in tandem with the charging MOSFET, Q_{12}. When the gate of Q_{12} is closed, allowing charging to occur, the gate on Q_5 also closes, shunting the output from Q_7 to ground. When the gate on Q_3 opens, the gate on Q_5 also opens and the signal from Q_7 is sent to the reset transistor Q_3. If the signal is low, the reset on the master-timer is held high and charging continues. If the signal is high, the RC delay (R_9 and C_3) continues to hold the gate closed on Q_5, allowing charging to continue. The capacitor's charge leaks off slowly until the gate of Q_5 opens and the signal from the voltage comparator is sent to the reset transistor Q_3, disabling the timer. The diode, D_5, prevents the capacitor from discharging to ground.

4. Synchronization MOSFET

The gate of the synchronization MOSFET, Q_{11}, is driven by the output of the master-timer, Q_1, with the drain being connected to the output of V_{B2}'s voltage comparator, Q_8, and the gate of the slave-timer reset transistor, Q_4. The source is connected to ground. When Q_1's output is high, Q_{11} shunts

Q_2's output signal and reset voltage to ground, disabling the timer. When Q_1 is low, Q_{11}'s gate is open and, if the signal from the comparator Q_8 is high, Q_4's gate closes and the reset voltage on Q_2 is sent to ground. When Q_1 is still low and Q_8 goes low, the gate on Q_4 opens and the reset on Q_2 goes high, allowing charging to occur. Q_1 and Q_2 can never be high at the same time.

5. Additional EPS Components

The schottky diode symbol, D_9, in the BCR schematic represents the 17 parallel blocking diodes on the solar array panels. The schottky diode, D_{10}, prevents the BCR circuitry from operating during periods of eclipse. This diode, although not shown, should be two diodes in parallel to prevent an open circuit failure of the bus. The zener diode, Z_1, and the resistor, R_{17}, will limit the BCR's circuit voltage to 18.0 volts, the recommended limit, in the event the solar array voltage, immediately after eclipse, exceeds this value.

VI. POWER CONDITIONING SYSTEM (PCS)

A. POWER CONDITION CONSIDERATIONS

It would be an exercise in futility on the part of the author to propose a power conditioning system for subsystems which have not been tested or even fully designed. The microprocessor discussed below is the only subsystem with a specific power requirement. The following general recommendations are made concerning PANSAT's power conditioning:

- Nondissipative-type convertors, switch-mode, are the best choice for meeting subsystem power requirements. These convertors are low in mass and small in size. Their output voltage can be greater than, equal to, or less than the input voltage based on three different configurations: a buck, a buck-boost, and a boost. Switch-mode convertors offer higher efficiencies than dissipative, or linear, regulators. [Ref. 34:p. 117]
- PANSAT subsystems should have redundant convertors/ regulators to eliminate a single point of failure. The outputs of the convertors are tied together, with the primary convertor output voltage biased slightly higher than the secondary, or backup, convertor. The selected

convertor should be capable of remote sensing where, via a voltage divider, feedback from the load is provided to the convertor. The voltage dividers can be used to trim the bias between the primary and secondary convertors.

B. MICROPROCESSOR POWER CONDITIONING

The microprocessor requires 2.6 watts of power at +5 volts. A suitable dc-dc convertor, which provides 0.2% load regulation and 0.1% line regulation, is the Mil-Spec 1300 series manufactured by Computer Products/Tecnectics. This convertor operates over a wide input voltage, 5-48 volts, and the output voltage can be adjusted from 5-24 volts. The convertor is rated at 3 watts and has an operating temperature of -55°C to 100°C. Remote sensing and short circuit protection are standard features. [Ref. 47:D-1672]

A possible arrangement for connecting the redundant switch-mode convertors is shown in Figure 16. Schottky diodes with a nominal forward voltage drop of 0.3 volts are used. The output voltage of the primary convertor is 5.1 volts after the diode voltage drop. The output of the second convertor is biased slightly lower at 5.0 volts. When the primary convertor is functioning, the second convertor's diode is reverse-biased. If the primary convertor fails, the diode on the secondary convertor becomes forward-biased and the regulator begins supplying the load demand. The voltage

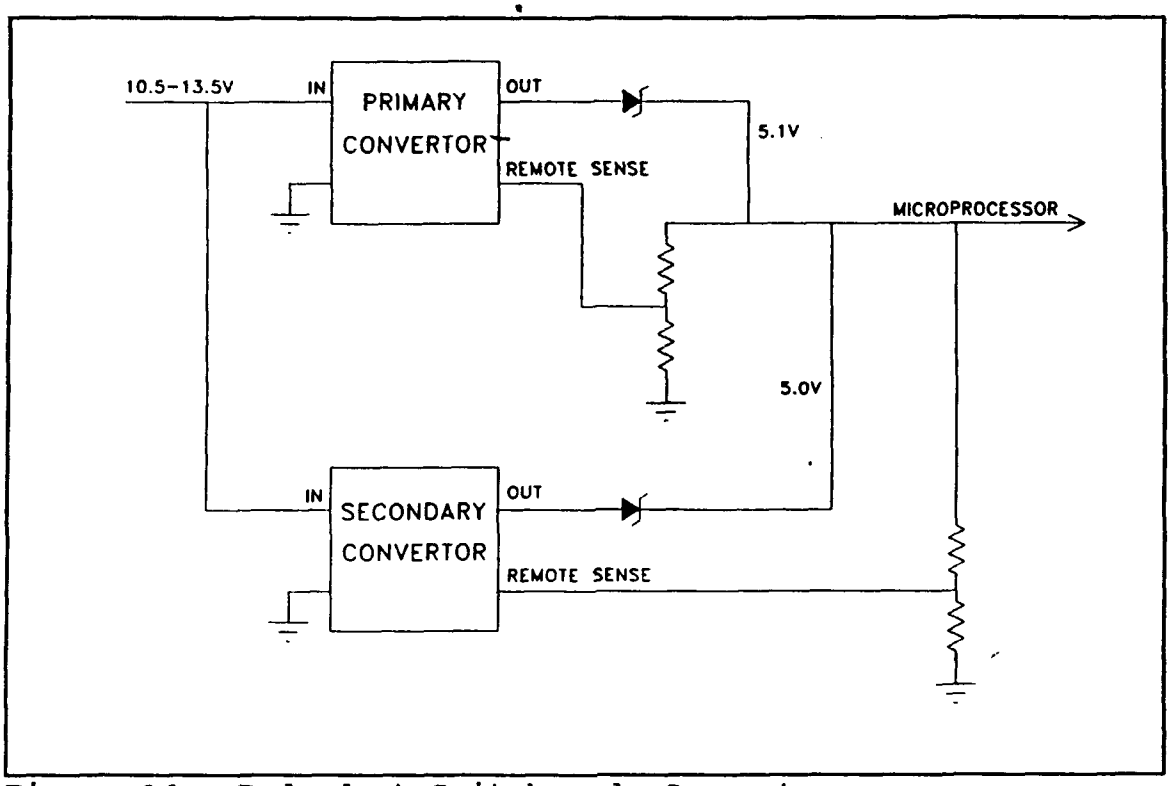

Figure 16. Redundant Switch-mode Convertors

dividers are connected to the remote sensing adjustment on each convertor. The experimental payload can use the output of these convertors if the power requirement of the payload is less than 0.4 watts.

VII. PROTOTYPE BCR TEST AND EVALUATION

A. TEST AND EVALUATION OBJECTIVES

Cost and time did not permit building a preliminary model of PANSAT's EPS. Instead, a breadboard model of the BCR circuitry was built along with two lead acid batteries. The objectives of the test and evaluation were:

- Validate the BCR design.
- Validate the operating setpoint of 10.8 volts for the voltage comparators.
- Confirm manufacturer-provided data on the lead acid cells
- Determine the time required to recharge the batteries from 20% capacity with a charging current of 0.96 amperes, simulating the transmitter being off.

B. ARTIFICIALITIES OF TEST ENVIRONMENT

The prototype BCR was tested under the following modified conditions:

- The solar array panel voltage was simulated using a constant 13.7 volt dc power supply, after D_1, as supply voltage for the BCR circuit.
- A variable coil resistor was used to simulate various satellite loads.

- The tests were conducted at ambient room temperature (25°C).
- A 13.5 volt dc power supply was used to simulate the distribution bus voltage, after D_{10}, for battery charging.
- The input for the temperature sensor, pin 3, on the MAXIM 673 precision reference voltage sources as not connected.
- A 2N7000 pure-enhancement N-channel MOSFET was used for Q_3, Q_4, Q_5, Q_6, and Q_{11}.
- Components were commercial-grade and not military rated.
- Non-precision resistors and capacitors were used.
- A dual knife-switch was used to switch the batteries from the BCR to load.
- Components D_1, D_{10}, Z_1, and R_{17} were not used.

The type of components and their actual values are listed in Appendix B.

C. TEST RESULTS

The BCR performed as predicted. The master-timer had a pulse period of 0.650 seconds vice a predicted value of 0.617. Similarly, the slave-timer had a pulse period of 0.660 seconds which exceeded the predicted value of 0.616. The increase in pulse periods are the result of a slight delay induced by the

steering diodes in each timing circuit. Figure 17 is a photograph of the two output waveforms of the timers. The top trace of Figure 17 is the master-timer waveform and the bottom trace is the slave-timer waveform. Scaling is 1 volt per division at 0.1 seconds per division. Figure 17 shows that when the master-timer output is high, the slave-timer is low and vice-versa. Figure 18 is a photograph of the two timer waveforms added together. Scaling in the photograph is 1 volt per division and 0.1 seconds per division. Any overlap between the waveforms would have created spiking which is not evident. The fraction of the waveform when both outputs of the two timers are zero is the dead-time between clock pulses. This value was measured as 0.04 seconds.

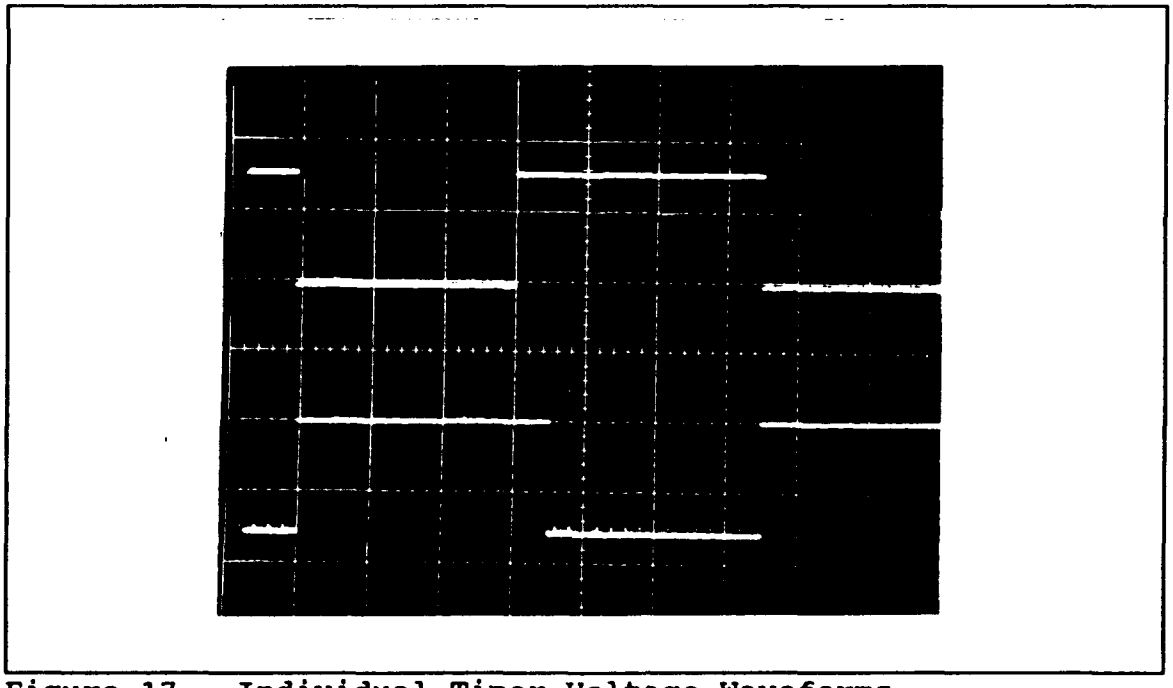

Figure 17. Individual Timer Voltage Waveforms

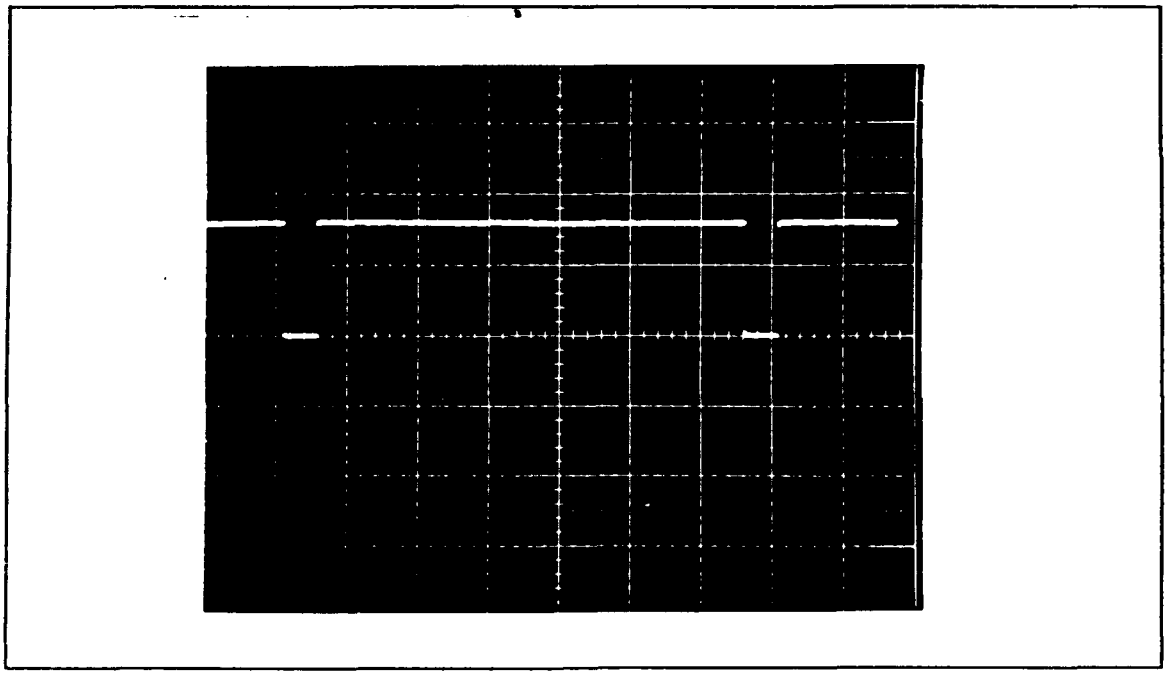

Figure 18. Sum of Timer Voltage Waveforms

Figure 19 is a photograph of the battery and voltage comparator waveforms for the master-timer's battery. The upper waveform of Figure 19 is the battery voltage at 1 volt per division and the bottom waveform is the output of the voltage comparator at 0.1 volts per division and 0.5 seconds per division. The voltage peaks in the battery's waveform indicate the charging MOSFET is closed, allowing the battery to charge. Simultaneously, in the lower waveform, the voltage comparator senses the high battery voltage and sends an erroneous high signal to secure battery charge, but the shunt transistor shunts this signal to ground and charging continues. In Figure 19, when the battery voltage waveform goes low, the comparator senses the true condition of the

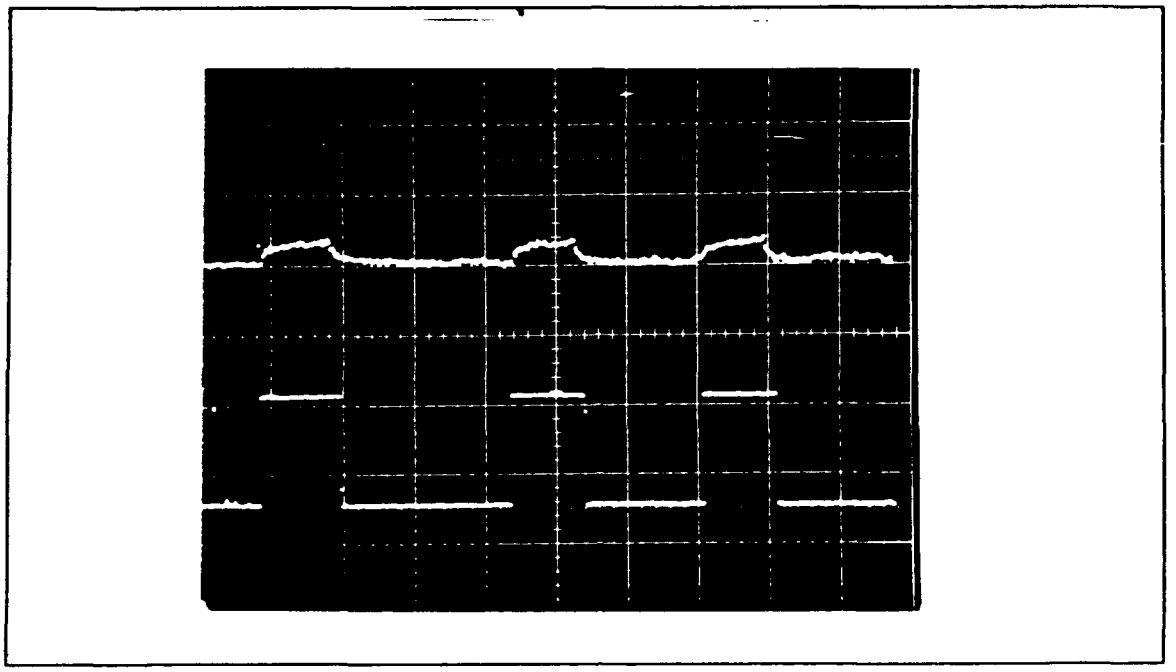

Figure 19. Battery and Voltage Comparator Waveforms

battery and sends a low signal indicating the battery still requires charging.

A setpoint of 10.7 volts was determined to be the best setpoint for the comparators. A higher setpoint voltage caused cyclic instability in the circuit. The battery voltage would drop, because of self-discharge, almost immediately and the comparator would activate the charging circuit. A lower setpoint was found to minimize this instability. The setpoint will probably change with new cells. The batteries used were obtained from the military supply system and were one year beyond the shelf-life expiration date. Additionally, the cells were repeatedly discharged over their entire capacity to simulate satellite load demands.

The X-cell lead acid batteries performed satisfactorily. The open circuit voltage of a cell was slightly less, by 0.03 volts, then the manufacturer's claim of 2.18 volts. However, the guaranteed voltage of 2.1 volts, at 5 amperes, was verified despite repeated cycles of discharging and charging over the cell's full capacity.

The time to recharge the batteries from a battery voltage of 10.0 volts, for both batteries, to near full capacity was approximately fourteen hours using a setpoint of 10.7 volts for the voltage comparators. This was two hours greater than expected but can be attributed to the degraded conditions of the batteries.

VIII. IMPROVEMENTS ON EPS PERFORMANCE

A. BCR EFFICIENCY

A slight increase in BCR efficiency can be achieved by reducing the dead-time between clock pulses of the two timers. Assuming a duty cycle of 48% and a pulse period of 0.625 seconds for each timer, the total dead-time is 0.05 seconds for 1.25 seconds. Increasing the duty cycle for each timer to 49.5% leaves a total dead-time of 0.0125 seconds for the combined pulse periods. The percent of total charging is increased from 96% to 99%. The efficiency of the BCR, η, is increased for a 58 minute charging period, with the transmitter off, by

$$\eta = \frac{0.99}{0.96} = 1.03 \qquad (8.1)$$

Therefore, a 3% increase in BCR efficiency (1.8 minutes of charging time) can be obtained by decreasing the tolerance on the timing circuit. This assumes that timing errors will not occur over varying operating temperatures.

B. TWO-AXIS STABILIZATION

PANSAT's power budget could be reduced and the solar array's output increased by using a rudimentary attitude-control system to passively stabilize the satellite. The

passive system consists of bar magnets mounted in the satellite which aligns the satellite's axis, normal to the baseplate panel, along the earth's magnetic field. Permalloy hysteresis damping rods, perpendicular to the primary magnet, reduces the spin about this axis. There are two advantages to using two-axis stabilization:

- PANSAT's antennas would not have to be omnidirectional thereby reducing the power required for communications.
- The baseplate panel will remain orientated towards the earth and not reduce the power generating capability of the array, since rotation would be about the baseplate panel. The average effective surface area for the solar array would be 1277 cm^2 (Table 5).

OSCAR's 6, 7, and 8 successfully used this method of attitude stabilization. The integration of the magnets requires no modification to the PANSAT except relocation of the omnidirectional antennas. [Ref. 48:p. 12-10]

C. SEQUENTIAL SHUNT REGULATOR

Another way to improve PANSAT's EPS is to optimize the available power using a shunt regulator. The shunt regulator maintains the bus voltage at a fixed value, irrespective of the changes in load and solar array temperature, by shunting excess current from the solar array. During eclipse the bus voltage is clamped at the battery voltage. Figure 20 is a block schematic of this configuration which is essentially the

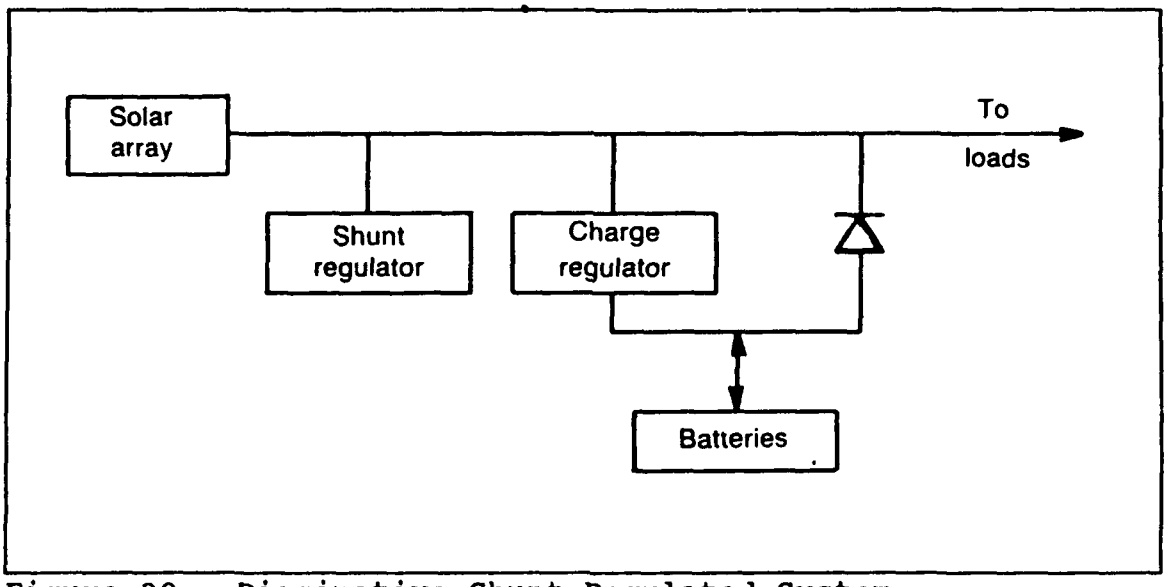

Figure 20. Dissipative Shunt Regulated System [From Ref. 34]

regulated sunlight bus mentioned in Chapter II. It is further classified as a dissipative system since the shunt regulator dissipates the unused portion of solar array power [Ref. 34:p. 115].

There are three types of shunt regulators that could be used for PANSAT's EPS: analog/linear, pulse-width modulated (PWM), and digital-shunt. Although the PWM and digital-shunt devices are more efficient and weigh less than an analog/linear regulator, they are more complex and are suitable for more sophisticated spacecraft. A sequential linear shunt regulator is appropriate for PANSAT because of its relative simplicity. It also responds quickly to output load and input voltage changes. Where a linear shunt regulator uses a single switch and resistor to dissipate excess energy, the sequential linear shunt regulator uses a

series of switches and resistors. Figure 21 depicts a simplified version of a sequential linear shunt regulator using bipolar junction transistors. The distribution bus voltage is scaled down and compared to a reference voltage. The difference between the two signals is input to a sequential drive control which controls the current through the sequential shunt stages by opening or closing the power transistors. Only one transistor conducts at a given time and excess solar array power is dissipated in the selected power transistor and resistor. The reference voltage used by the sequential drive control to drive the difference or error signal usually corresponds to bus voltage at maximum power of the solar array at EOL. A more efficient variation is to change the reference voltage over the satellite's lifetime, accounting for degradation of the solar array. [Ref. 34:p. 120]

D. GALLIUM ARSENIDE CELLS

The solar array's power output can be increased by using GaAs cells. The primary advantages of GaAs cells are higher efficiency and reduced temperature dependency [Ref. 49:p. 23]. Although these cells were ruled out as too expensive in the preliminary design, there is always the possibility of obtaining surplus cells. Table 13 lists some of the bare cell parameters for a typical production GaAs cell [Ref. 50:p. 9]. Since a GaAs cell generates twice the voltage of a silicon

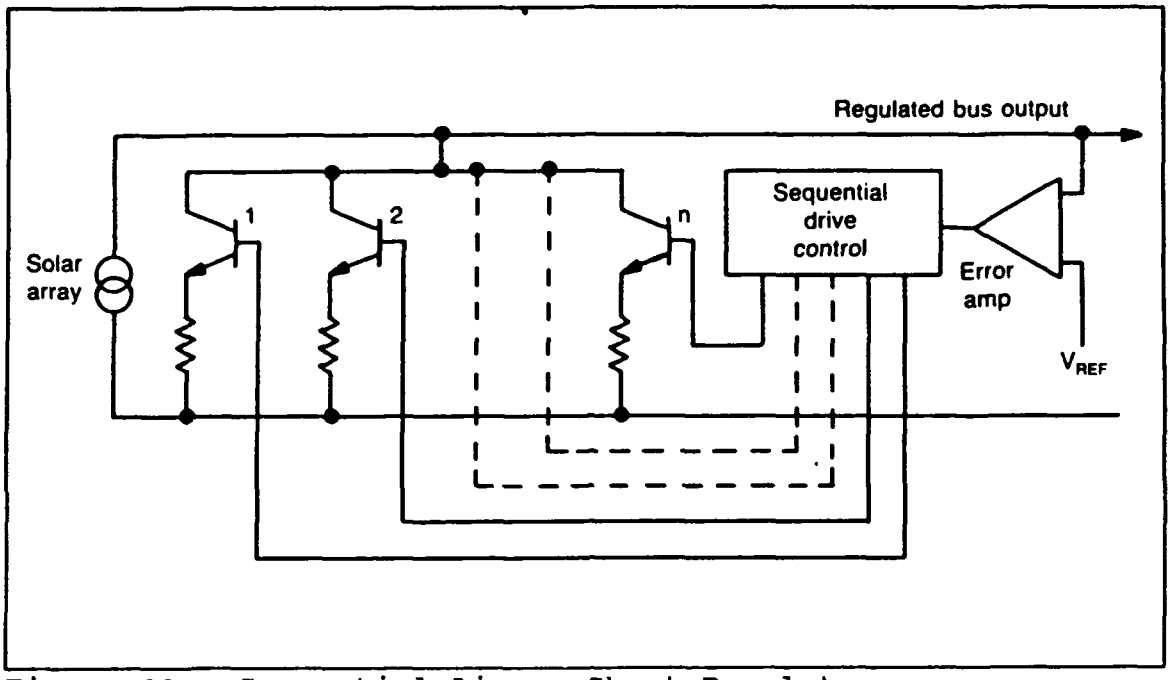

Figure 21. Sequential Linear Shunt Regulator [From Ref. 34]

cell, PANSAT's solar cell arrangement on each panel will have to be modified. Instead of a single string of 32 cells, the GaAs cells should be arranged in two strings of 16 cells, in series, per panel. These two strings should be connected in parallel with the remaining 16 solar panels for a total of 34 strings of cells. The panel voltage at 28°C, after the blocking diode, will be approximately 15.7 volts and the distribution bus voltage will be approximately 15.4 volts. A voltage limiter may be required for battery charging.

TABLE 13. GAAS BARE CELL PARAMETERS (5 MIL)

PARAMETER (1 AM0 @ 28°C)	DIMENSION (5 MIL)	UNIT
Open circuit voltage (V_{oc})	1012.5	mV
Short circuit current (I_{sc})	258.4	mA
Optimum bias voltage (V_{mp})	971.5	mV
Optimum bias current (I_{mp})	242.4	mA
Base Resistivity	0.5	Ohm-cm
Conversion efficiency	18.4	%
Max power output (V_{MP})	235.5	mW
Cell area	2 x 4	cm^2
Cell thickness	0.001	mm
Cell weight	1.6	gm/cm^3

The increase in solar array performance can be examined by calculating the GaAs solar cell output, using Equation 3.4, and comparing it to the power output from K6700 silicon cells. The power generated from a GaAs cell at BOL is defined by

$$P_c(BOL) = (P_o)(S')(F_{T(op)})(F_m)(F_{sh})(F_{BD})(F_{CONF}) \qquad (3.4)$$

where

P_o = 0.2496 W (From Table 13),

S' = 0.967 (From Chapter III),

$F_{T(op)}$ = GaAs cell's temperature degradation factor,

F_M = 0.99 (From Chapter III),

F_{SH} = 1.0 (From Chapter III),

F_{BD} = 0.94 (From Chapter III), and

F_{CONF} = 1.0 (From Chapter III).

The parameter $F_{T(op)}$ for GaAs cells is small compared to silicon cells. The degradation is 0.033%/°C [Ref. 49:p. 16]. Therefore, $F_{T(op)}$ for PANSAT's GaAs has an assumed value of 0.95. Substituting the above values into Equation 3.4, the power generated by a single GaAs cell at BOL is

$$P_{C(BOL)}=(249.6)(.967)(.97)(.99)(1)(.94)(1) \qquad (8.2)$$

$$P_{C(BOL)} = 0.2013 \text{ W}$$

The solar array power output, at BOL, is

$$P_{BOL} = P_{C(BOL)}\left(\frac{A_{EFF}}{A_c}\right) \qquad (3.19)$$

where

$A_{EFF} = 1145 \text{ cm}^2$,

$A_C = 2 \times 4 \text{ cm}^2$, and

$P_{C(BOL)} = 0.2013$ W.

Substituting and solving for P_{BOL}

$$P_{BOL} = 0.2013\left(\frac{1145}{8}\right) = 28.8 \text{ W} \qquad (8.3)$$

The increase in the solar array power generating capability is expressed as

$$P_{out} = \frac{GaAs_{BOL}}{K6700_{BOL}} = \frac{28.8w}{18.3w} = 1.57 \qquad (8.4)$$

A power gain of 57% is achieved by using GaAs cells. There are considerable differences, beyond the scope of this thesis, between GaAs and silicon solar cells which should be fully examined before selecting GaAs cells for PANSAT.

IX. RECOMMENDATIONS AND CONCLUSION

A. RECOMMENDATIONS

It should be stressed that the design presented in this thesis is preliminary and does not represent a flight model or even a prototype flight model. Many areas of the EPS still need to be addressed before solidifying the design of a prototype flight model. Due to the large scope of designing an EPS, the next phase of EPS design should be broken into two separate thesis topics for further investigation. These topics, solar array and EPS electronics, should address the following, noninclusive, areas.

1. Areas of Investigation for the Solar Array

- Test and evaluation of a complete solar panel under simulated conditions in NPS's solar laboratory.
- Simulation of the loss of multiple solar panels and the effect on bus voltage.
- Computer modeling of the solar array output based on PANSAT's orbit, the seasonal variations in solar flux, solar cell degradation due to radiation, and satellite rate of tumbling.

- Investigation of the possibility of a PANSAT power system lock-up, including corrective measures required.
- Study of specific hardware requirements and assembly procedure for the solar panels.

2. Areas of Investigation for EPS Electronics

- Further development of the BCR, batteries, and the dc-dc convertors including environmental testing.
- Determination of over-current protective measures.
- Continuation of efforts to identify possible single points of failure in the EPS.
- Determination of sensor locations and select temperature, voltage, and current sensors for telemetry purposes.
- Integration of EPS with PANSAT's microprocessor.
- Study of a design method of transmitter lockout to prevent battery capacity from being exhausted due to overuse.
- Determination of the role ground-controllers will have, if any, in operating the EPS.

B. CONCLUSION

This thesis has presented a practical preliminary design for the PANSAT EPS. The BCR portion of the design was tested and proven to work. Additional proposals, at the expense of

cost or complexity, were made to increase the output or efficiency of the EPS. Prior to further modification or design of the EPS, the other spacecraft subsystems (communications, microprocessor, thermal control and experimental payload) should be brought to a reasonable level of maturity and their power requirements reevaluated. After reevaluation, if the power budget is negative, then some subsystems, probably the transmitter, will require redesign until a positive budget is attained. An alternative is to accept a negative power budget, along with a greater DOD on the batteries, and periodically restrict satellite operations until the batteries are recharged. Finally, reliability and simplicity should be the tantamount criteria in designing the PANSAT.

APPENDIX A - EFFECTIVE SURFACE AREA PROGRAM

```
**        THIS PROGRAM COMPUTES THE EFFECTIVE SURFACE AREA,
AEFF, OF PANSAT'S SOLAR ARRAY USING THE ROTATION ANGLE ABOUT
THE Z-AXIS AS THE INPUT VARIABLE.


 1        INTEGER S(17,3), T
**        S(17,3) ARE SURFACE VECTORS AND T IS TIME

 2        REAL E(3), AEFF,APRIME,DEG,THETA,NS(17,3)
**        E(3) IS THE VECTOR FROM THE SATELLITE TO THE SUN
**        AEFF IS THE EFFECTIVE AREA, WITH APRIME THE BUFFER
**        DEG IS THE ANGLE MADE IN TIME, T.
**        THETA IS THE ROTATION ABOUT Z, AND NS(17,3) ARE THE
**        NEW SURFACE VECTORS.

 3        OPEN(UNIT=1,STATUS='NEW',ACCESS='SEQUENTIAL',
         FILE='FLUX')
 4        APRIME = 0.00

**        INITIALIZE THE VARIABLES
 5        T = 0
 6        DO 20, I=1,17
 7        DO 10, J=1,3
 8          S(I,J) = 0
 9   10   CONTINUE
10   20   CONTINUE
11        AEFF = 0
12        DO 25,I=1,8
13          S(I,3) = 0
14   25   CONTINUE
15        DO 28, I=9,17
16        IF((I.GE.13).AND.(I.LE.16))THEN
17          S(I,3) =-181
18        ELSE
19          S(I,3) = 181
20        ENDIF
21   28   CONTINUE
**        SURFACE VECTOR COMPONENTS ARE AS FOLLOWS

22        S(1,1)=256
23        S(2,1)=181
24        S(2,2)=181
25        S(3,2)=256
```

```
      S(4,1)=-181
      S(4,2)=181
      S(5,1)=-256
      S(6,1)=-181
      S(6,2)=-181
      S(7,2)=-256
      S(8,1)=181
      S(8,2)=-181
      S(9,1)=181
      S(10,2)=181
      S(11,1)=-181
      S(12,2)=-181
      S(13,1)=181
      S(14,2)=181
      S(15,1)=-181
      S(16,2)=-181
      S(17,3)= 256
      E(1) = 0.00
      E(2) = 1.00
      E(3) = 0.00
      PRINT, 'ENTER ROTATION ANGLE ABOUT THE Z-AXIS (DEG)'
      READ(5,*) THETA
      THETA = THETA*3.141593/180.
      WRITE(6,90) THETA
      DO 30,I=1,17
        NS(I,1) = COS(THETA)*S(I,1)+SIN(THETA)*S(I,2)
        NS(I,2) =-(SIN(THETA)*S(I,1))+COS(THETA)*S(I,2)
        NS(I,3) = S(I,3)
30    CONTINUE
      DO 45,I=1,17
      DO 40,J=1,3
        APRIME = NS(I,J)*E(J)
        IF(APRIME.GE.0)THEN
          AEFF = AEFF + APRIME
        ENDIF
40    CONTINUE
45    CONTINUE
      WRITE(1,80) T,AEFF,E(1),E(2),E(3)
      AEFF = 0
      DO 75,T=1,63
        DEG = T*0.1
        E(1)=0
        E(2)=COS(DEG)
        E(3)=SIN(DEG)
        DO 70,I=1,17
          DO 65,J=1,3
          APRIME=NS(I,J)*E(J)
          IF(APRIME.GE.0)THEN
            AEFF = AEFF + APRIME
          ENDIF
65        CONTINUE
```

```
77  70    CONTINUE
78        WRITE(1,80) T,AEFF,E(1),E(2),E(3)
79  80    FORMAT(1X,I2,4X,'AEFF:',1X,F7.2,2X,'E:',1X,F7.5,2X,
          F7.5,2X,F7.5)
80        AEFF = 0
81  75    CONTINUE
82  90    FORMAT(1X,'ANGLE OF ROTATION ABOUT Z IS ',F7.4,'
          RADIANS')
83        CLOSE(UNIT=1)
84        PRINT, TOTAL
85        STOP
86        END
```

APPENDIX B - BCR COMPONENTS

The following components and values were used to test the BCR schematic depicted in Figure 5.2:

V_{BUS} = 13.5 V
V_p = 13.8 V

R_1 = 0.92 MΩ
R_2 = 0.92 MΩ
R_3 = 1.00 MΩ
R_4 = 1.00 MΩ
R_5 = 1.0 KΩ
R_6 = 1.0 KΩ
R_7 = 4.0 MΩ
R_8 = 1.0 MΩ
R_9 = 18 MΩ
R_{10} = 4.0 MΩ
R_{11} = 1.0 MΩ
R_{12} = 18.0 MΩ
R_{13} = 1.14 MΩ (VARIABLE)
R_{14} = 1.0 MΩ
R_{15} = 1.14 MΩ (VARIABLE)
R_{16} = 1.0 MΩ

C_1 = 0.47 μF
C_2 = 0.47 μF
C_3 = 0.47 μF
C_4 = 0.47 μF

D_1 = 1N914
D_2 = 1N914
D_3 = 1N914
D_4 = 1N914
D_5 = 1N914
D_6 = 1N914
D_7 = IN5820
D_8 = IN5820

Q_1 = LCM7555
Q_2 = LCM7555
Q_3 = 2N7000
Q_4 = 2N7000
Q_5 = 2N7000
Q_6 = 2N7000
Q_7 = LT1017
Q_8 = LT1017
Q_9 = MAX673CPA
Q_{10} = MAX673CPA
Q_{11} = 2N7000
Q_{12} = RFH45N05
Q_{13} = RFH45N05

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